

QYH500

Library

Data

Sheet

- **Commercial**
- **Military**

Chip Express Corporation

Chip *Express*[®]

The ASIC Time-to-Market Solution™



QYH500

Library

Data

Sheet

— Commercial

Chip Express Corporation

ChipExpress®

The ASIC Time-to-Market Solution™

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Library Summary

Name	Page	Drive	Cells	Timing Information								Description
				tPLH (ns)		tPHL (ns)		ΔtPLH (ns/pF)		ΔtPHL (ns/pF)		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
AD2001	5-1	1	2	0.53	0.88	0.55	0.91	0.74	1.23	0.57	0.95	Z = A1*A2
AD2101	5-2	1	2	0.37	0.61	0.46	0.76	1.44	2.39	0.54	0.90	Z = A1*NOT BN
AD2002	5-3	2	2	0.61	1.01	0.62	1.03	0.38	0.63	0.32	0.53	Z = A1*A2
AD3001	5-4	1	2	0.78	1.29	0.67	1.11	0.75	1.24	0.58	0.96	Z = A1*A2*A3
AD3002	5-5	2	3	0.90	1.49	0.75	1.24	0.41	0.68	0.33	0.55	Z = A1*A2*A3
AD4001	5-6	1	3	1.12	1.86	0.79	1.31	0.78	1.29	0.60	1.00	Z = A1*A2*A3*A4
AD4002	5-7	2	3	1.24	2.06	0.83	1.38	0.43	0.71	0.35	0.58	Z = A1*A2*A3*A4
AD5001	5-8	1	3	1.53	2.54	0.89	1.48	0.81	1.34	0.62	1.03	Z = A1*A2*A3*A4*A5
AD6001	5-9	1	4	0.96	1.59	0.75	1.24	1.44	2.39	0.58	0.96	Z = A1*A2*A3*A4*A5*A6
AD7001	5-10	1	5	1.26	2.09	0.85	1.41	1.43	2.37	0.60	1.00	Z = A1*A2*A3*A4*A5*A6*A7
AD8001	5-11	1	5	1.26	2.09	0.84	1.39	1.43	2.37	0.60	1.00	Z = A1*A2*A3*A4*A5*A6*A7*A8
EN2001	5-12	1	3	0.66	1.10	0.83	1.38	0.74	1.23	0.63	1.05	Z = NOT(A1∞A2)
EN2002	5-13	2	4	0.66	1.10	1.06	1.76	0.38	0.63	0.40	0.66	Z = NOT(A1∞A2)
EN3001	5-14	1	6	1.65	2.74	2.13	3.54	0.74	1.23	0.64	1.06	Z = NOT(A1∞A2∞A3)
EX2001	5-15	1	3	0.88	1.46	1.07	1.78	0.75	1.24	0.57	0.95	Z = A1∞A2
EX2002	5-16	2	4	0.94	1.56	1.12	1.86	0.40	0.66	0.33	0.55	Z = A1∞A2
EX3001	5-17	1	6	2.01	3.34	2.08	3.45	0.75	1.24	0.57	0.95	Z = A1∞A2∞A3
IT1001	5-18	1	4	0.72	1.20	0.76	1.26	0.75	1.24	0.62	1.03	Inverting 3-state buffer the enable input is active low
IT1002	5-19	2	5	0.81	1.34	0.82	1.36	0.40	0.66	0.40	0.66	Inverting 3-state buffer the enable input is active low
IT1004	5-20	4	7	0.89	1.48	1.00	1.66	0.26	0.43	0.30	0.50	Inverting 3-state buffer the enable input is active low
IT1101	5-21	1	4	0.53	0.88	1.00	1.66	0.75	1.24	0.61	1.01	Inverting 3-state buffer the enable input is active high
IT1102	5-22	2	5	0.58	0.96	1.07	1.78	0.40	0.66	0.40	0.66	Inverting 3-state buffer the enable input is active high
IT1104	5-23	4	7	0.66	1.10	1.24	2.06	0.26	0.43	0.30	0.50	Inverting 3-state buffer the enable input is active high
IV1001	5-24	1	1	0.13	0.22	0.22	0.37	0.74	1.23	0.54	0.90	Z = NOT A
IV1002	5-25	2	1	0.15	0.25	0.22	0.37	0.36	0.60	0.27	0.45	Z = NOT A
IV1003	5-26	3	2	0.15	0.25	0.20	0.33	0.24	0.40	0.19	0.32	Z = NOT A
IV1004	5-27	4	2	0.15	0.25	0.19	0.32	0.18	0.30	0.15	0.25	Z = NOT A
IV1005	5-28	5	3	0.15	0.25	0.18	0.30	0.14	0.23	0.13	0.22	Z = NOT A
IV1006	5-29	6	3	0.13	0.22	0.18	0.30	0.12	0.20	0.11	0.18	Z = NOT A
IV1007	5-30	7	4	0.13	0.22	0.16	0.27	0.10	0.17	0.10	0.17	Z = NOT A
IV1008	5-31	8	4	0.13	0.22	0.22	0.37	0.09	0.15	0.07	0.12	Z = NOT A
IV1010	5-32	10	5	0.13	0.22	0.20	0.33	0.07	0.12	0.05	0.08	Z = NOT A
IV1020	5-33	20	10	0.13	0.22	0.18	0.30	0.03	0.05	0.03	0.05	Z = NOT A
IV1030	5-34	30	15	0.13	0.22	0.19	0.32	0.02	0.03	0.02	0.03	Z = NOT A
ND2001	5-35	1	1	0.23	0.38	0.28	0.46	0.75	1.24	0.92	1.53	Z = NOT(A1*A2)
ND2101	5-36	1	2	0.37	0.61	0.36	0.60	0.76	1.26	0.97	1.61	Z = NOT(A1*NOT BN)
ND2002	5-37	2	2	0.23	0.38	0.28	0.46	0.37	0.61	0.46	0.76	Z = NOT(A1*A2)
ND3001	5-38	1	2	0.32	0.53	0.45	0.75	0.75	1.24	1.30	2.16	Z = NOT(A1*A2*A3)
ND3002	5-39	2	3	0.32	0.53	0.45	0.75	0.38	0.63	0.65	1.08	Z = NOT(A1*A2*A3)
ND3101	5-40	1	2	0.40	0.66	0.45	0.75	0.76	1.26	1.31	2.17	Z = NOT(A1*A2*NOT BN)
ND4001	5-41	1	2	0.40	0.66	0.72	1.20	0.77	1.28	1.69	2.81	Z = NOT(A1*A2*A3*A4)
ND4002	5-42	2	4	0.37	0.61	0.70	1.16	0.40	0.66	0.84	1.39	Z = NOT(A1*A2*A3*A4)
ND5001	5-43	1	3	0.43	0.71	1.02	1.69	0.80	1.33	2.07	3.44	Z = NOT(A1*A2*A3*A4*A5)
ND5002	5-44	2	5	0.42	0.70	1.02	1.69	0.41	0.68	1.05	1.74	Z = NOT(A1*A2*A3*A4*A5)

Name	Page	Drive	Cells	Timing Information								Description
				tPLH (ns)		tPHL (ns)		ΔtPLH (ns/pF)		ΔtPHL (ns/pF)		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
ND6001	5-45	1	5	0.85	1.41	1.37	2.27	0.75	1.24	0.59	0.98	Z = NOT(A1*A2*A3*A4*A5*A6)
ND6002	5-46	2	5	0.96	1.59	1.52	2.52	0.37	0.61	0.36	0.60	Z = NOT(A1*A2*A3*A4*A5*A6)
ND7001	5-47	1	5	0.97	1.61	1.67	2.77	0.74	1.23	0.60	1.00	Z = NOT(A1*A2*A3*A4*A5*A6*A7)
ND7002	5-48	2	6	1.05	1.74	1.80	2.99	0.37	0.61	0.36	0.60	Z = NOT(A1*A2*A3*A4*A5*A6*A7)
ND8001	5-49	1	6	0.97	1.61	1.67	2.77	0.74	1.23	0.60	1.00	Z = NOT(A1*A2*A3*A4*A5*A6*A7*A8)
ND8002	5-50	2	6	1.06	1.76	1.83	3.04	0.37	0.61	0.36	0.60	Z = NOT(A1*A2*A3*A4*A5*A6*A7*A8)
NR2001	5-51	1	1	0.34	0.56	0.28	0.46	1.43	2.37	0.55	0.91	Z = NOT(A1+A2)
NR2101	5-52	1	2	0.37	0.61	0.46	0.76	1.44	2.39	0.54	0.90	Z = NOT(A1+NOT BN)
NR2002	5-53	2	2	0.34	0.56	0.26	0.43	0.72	1.20	0.28	0.46	Z = NOT(A1+A2)
NR3001	5-54	1	2	0.67	1.11	0.31	0.51	2.14	3.55	0.57	0.95	Z = NOT(A1+A2+A3)
NR3002	5-55	2	3	0.65	1.08	0.29	0.48	1.07	1.78	0.29	0.48	Z = NOT(A1+A2+A3)
NR3101	5-56	1	2	0.46	0.76	0.46	0.76	2.15	3.57	0.54	0.90	Z = NOT(A1+A2+NOT BN)
NR4001	5-57	1	2	1.18	1.96	0.32	0.53	2.83	4.70	0.58	0.96	Z = NOT(A1+A2+A3+A4)
NR4002	5-58	2	4	1.16	1.93	0.31	0.51	1.42	2.36	0.30	0.50	Z = NOT(A1+A2+A3+A4)
NR5001	5-59	1	3	1.77	2.94	0.34	0.56	3.54	5.88	0.59	0.98	Z = NOT(A1+A2+A3+A4+A5)
NR5002	5-60	2	5	1.73	2.87	0.32	0.53	1.77	2.94	0.30	0.50	Z = NOT(A1+A2+A3+A4+A5)
NR6001	5-61	1	5	1.53	2.54	0.89	1.48	0.75	1.24	0.57	0.95	Z = NOT(A1+A2+A3+A4+A5+A6)
NR6002	5-62	2	5	1.65	2.74	0.97	1.61	0.38	0.63	0.31	0.51	Z = NOT(A1+A2+A3+A4+A5+A6)
NR7001	5-63	1	5	2.20	3.65	0.94	1.56	0.75	1.24	0.57	0.95	Z = NOT(A1+A2+A3+A4+A5+A6+A7)
NR7002	5-64	2	6	2.33	3.87	1.01	1.68	0.40	0.66	0.31	0.51	Z = NOT(A1+A2+A3+A4+A5+A6+A7)
NR8001	5-65	1	6	2.18	3.62	0.93	1.54	0.75	1.24	0.57	0.95	Z = NOT(A1+A2+A3+A4+A5+A6+A7+A8)
NR8002	5-66	2	6	2.31	3.83	1.01	1.68	0.40	0.66	0.31	0.51	Z = NOT(A1+A2+A3+A4+A5+A6+A7+A8)
NT1001	5-67	1	4	0.70	1.16	0.75	1.24	0.75	1.24	0.62	1.03	3-state buffer the enable input is active low
NT1002	5-68	2	5	0.81	1.34	0.81	1.34	0.40	0.66	0.40	0.66	3-state buffer the enable input is active low
NT1004	5-69	4	7	0.89	1.48	0.99	1.64	0.26	0.43	0.30	0.50	3-state buffer the enable input is active low
NT1101	5-70	1	4	0.52	0.86	0.99	1.64	0.75	1.24	0.61	1.01	3-state buffer the enable input is active high
NT1102	5-71	2	5	0.58	0.96	1.07	1.78	0.40	0.66	0.40	0.66	3-state buffer the enable input is active high
NT1104	5-72	4	7	0.66	1.10	1.25	2.07	0.26	0.43	0.29	0.48	3-state buffer the enable input is active high
NV1001	5-73	1	1	0.35	0.58	0.39	0.65	0.74	1.23	0.55	0.91	Z = A
NV1002	5-74	2	2	0.41	0.68	0.47	0.78	0.37	0.61	0.30	0.50	Z = A
NV1003	5-75	3	2	0.47	0.78	0.58	0.96	0.25	0.41	0.22	0.37	Z = A
NV1004	5-76	4	3	0.41	0.68	0.46	0.76	0.19	0.32	0.16	0.27	Z = A
NV1005	5-77	5	4	0.43	0.71	0.48	0.80	0.15	0.25	0.14	0.23	Z = A
NV1006	5-78	6	4	0.46	0.76	0.54	0.90	0.13	0.22	0.13	0.22	Z = A
NV1007	5-79	7	5	0.42	0.70	0.46	0.76	0.11	0.18	0.10	0.17	Z = A
NV1008	5-80	8	6	0.41	0.68	0.47	0.78	0.09	0.15	0.07	0.12	Z = A
NV1010	5-81	10	7	0.43	0.71	0.53	0.88	0.07	0.12	0.06	0.10	Z = A
NV1020	5-82	20	13	0.48	0.80	0.58	0.96	0.04	0.07	0.03	0.05	Z = A
NV1030	5-83	30	19	0.53	0.88	0.61	1.01	0.02	0.03	0.02	0.03	Z = A
OR2001	5-84	1	2	0.43	0.71	0.78	1.29	0.75	1.24	0.60	1.00	Z = A1+A2
OR2101	5-85	1	2	0.37	0.61	0.36	0.60	0.76	1.26	0.97	1.61	Z = A1+NOT BN
OR2002	5-86	2	2	0.52	0.86	0.90	1.49	0.37	0.61	0.36	0.60	Z = A1+A2
OR3001	5-87	1	2	0.47	0.78	1.29	2.14	0.75	1.24	0.67	1.11	Z = A1+A2+A3
OR3002	5-88	2	3	0.54	0.90	1.43	2.37	0.38	0.63	0.42	0.70	Z = A1+A2+A3
OR4001	5-89	1	3	0.53	0.88	1.94	3.22	0.76	1.26	0.76	1.26	Z = A1+A2+A3+A4
OR4002	5-90	2	3	0.58	0.96	2.14	3.55	0.40	0.66	0.49	0.81	Z = A1+A2+A3+A4
OR5001	5-91	1	3	0.54	0.90	2.65	4.40	0.77	1.28	0.85	1.41	Z = A1+A2+A3+A4+A5
OR6001	5-92	1	4	0.59	0.98	1.33	2.21	0.75	1.24	0.95	1.58	Z = A1+A2+A3+A4+A5+A6
OR7001	5-93	1	5	0.61	1.01	1.98	3.29	0.76	1.26	0.98	1.63	Z = A1+A2+A3+A4+A5+A6+A7

Name	Page	Drive	Cells	Timing Information								Description
				tPLH (ns)		tPHL (ns)		ΔtPLH (ns/pF)		ΔtPHL (ns/pF)		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
OR8001	5-94	1	5	0.61	1.01	1.98	3.29	0.76	1.26	0.98	1.63	Z = A1+A2+A3+A4+A5+A6+A7+A8
AN3121	6-1	1	2	0.48	0.80	0.34	0.56	1.45	2.41	0.57	0.95	Z = NOT(A1*A2+B1)
AN4121	6-2	1	2	0.72	1.20	0.37	0.61	1.49	2.47	0.57	0.95	Z = NOT(A1*A2*A3+B1)
AN4131	6-3	1	2	1.02	1.69	0.36	0.60	2.07	3.44	0.58	0.96	Z = NOT(A1*A2+B1+B2)
AN4221	6-4	1	2	0.52	0.86	0.48	0.80	1.08	1.79	0.93	1.54	Z = NOT(A1*A2+B1*B2)
AN5121	6-5	1	3	0.90	1.49	0.39	0.65	1.51	2.51	0.60	1.00	Z = NOT(A1*A2*A3+A4+B1)
AN5231	6-6	1	3	0.93	1.54	0.37	0.61	1.79	2.97	0.60	1.00	Z = NOT(A1*A2+B1*B2+C1)
AN6221	6-7	1	3	0.43	0.71	0.52	0.86	0.97	1.61	1.30	2.16	Z = NOT(A1*A2*A3+B1*B2*B3)
AN6331	6-8	1	3	0.43	0.71	0.35	0.58	1.41	2.34	0.92	1.53	Z = NOT(A1*A2+B1*B2+C1*C2)
AN8221	6-9	1	4	0.53	0.88	0.77	1.28	0.93	1.54	1.69	2.81	Z = NOT(A1*A2*A3*A4+B1*B2*B3*B4)
AN8441	6-10	1	4	0.53	0.88	0.39	0.65	1.76	2.92	0.92	1.53	Z = NOT(A1*A2+B1*B2+C1*C2+D1*D2)
AO3121	6-11	1	2	0.54	0.90	0.96	1.59	0.75	1.24	0.75	1.24	Z = A1*A2+B1
AO4122	6-12	2	3	0.67	1.11	1.44	2.39	0.40	0.66	0.42	0.70	Z = A1*A2*A3+B1
AO4132	6-13	2	3	0.65	1.08	1.70	2.82	0.38	0.63	0.80	1.33	Z = A1*A2+B1+B2
AO4222	6-14	2	3	0.65	1.08	0.85	1.41	0.40	0.66	0.36	0.60	Z = A1*A2+B1*B2
AO5121	6-15	1	3	0.67	1.11	1.60	2.66	0.77	1.28	0.73	1.21	Z = A1*A2*A3*A4+B1
AO5231	6-16	1	3	0.60	1.00	1.54	2.56	0.76	1.26	0.74	1.23	Z = A1*A2+B1*B2+C1
AO6222	6-17	2	4	0.96	1.59	0.96	1.59	0.41	0.68	0.37	0.61	Z = A1*A2*A3+B1*B2*B3
AO6332	6-18	2	4	0.70	1.16	1.12	1.86	0.40	0.66	0.41	0.68	Z = A1*A2+B1*B2+C1*C2
AO8222	6-19	2	5	1.32	2.19	1.03	1.71	0.43	0.71	0.38	0.63	Z = A1*A2*A3*A4+B1*B2*B3*B4
AO8442	6-20	2	5	0.72	1.20	1.26	2.09	0.40	0.66	0.46	0.76	Z = A1*A2+B1*B2+C1*C2+D1*D2
CX0011	6-21	1	3	0.67	1.11	0.66	1.10	0.77	1.28	0.99	1.64	Z = NOT((A1+A2)*NOT(B1*B2))
CX0021	6-22	1	3	0.78	1.29	0.93	1.54	1.49	2.47	0.64	1.06	Z = NOT(A1*A2+NOT(B1+B2))
CX0031	6-23	1	3	1.06	1.76	0.59	0.98	1.78	2.95	0.93	1.54	Minority voter Z = NOT((A*B)+(B*C)+(A*C))
CX0042	6-24	2	4	1.02	1.69	1.77	2.94	0.38	0.63	0.50	0.83	Majority voter Z = (A*B)+(B*C)+(A*C)
OA3121	6-25	1	2	0.62	1.03	0.62	1.03	0.74	1.23	0.74	1.23	Z = (A1+A2)*B1
OA4122	6-26	2	3	0.81	1.34	0.83	1.38	0.41	0.68	0.37	0.61	Z = (A1+A2+A3)*B1
OA4132	6-27	2	3	1.03	1.71	0.84	1.39	0.40	0.66	0.38	0.63	Z = (A1+A2)*B1*B2
OA4222	6-28	2	3	0.64	1.06	0.99	1.64	0.38	0.63	0.37	0.61	Z = (A1+A2)*(B1+B2)
OA5121	6-29	1	3	0.85	1.41	0.84	1.39	0.76	1.26	0.72	1.20	Z = (A1+A2+A3+A4)*B1
OA5231	6-30	1	3	0.84	1.39	0.96	1.59	0.78	1.29	0.62	1.03	Z = ((A1+A2)*(B1+B2))*C1
OA6222	6-31	2	4	0.65	1.08	1.60	2.66	0.40	0.66	0.44	0.73	Z = (A1+A2+A3)*(B1+B2+B3)
OA6332	6-32	2	4	0.77	1.28	1.05	1.74	0.40	0.66	0.38	0.63	Z = (A1+A2)*(B1+B2)*(C1+C2)
OA8222	6-33	2	5	0.66	1.10	2.31	3.83	0.40	0.66	0.52	0.86	Z = (A1+A2+A3+A4)*(B1+B2+B3+B4)
OA8442	6-34	2	5	0.89	1.48	1.09	1.81	0.42	0.70	0.40	0.66	Z = (A1+A2)*(B1+B2)*(C1+C2)*(D1+D2)
ON3121	6-35	1	2	0.31	0.51	0.32	0.53	0.76	1.26	0.97	1.61	Z = NOT((A1+A2)*B1)
ON4121	6-36	1	2	0.36	0.60	0.42	0.70	0.77	1.28	0.98	1.63	Z = NOT((A1+A2+A3)*B1)
ON4131	6-37	1	2	0.39	0.65	0.55	0.91	0.77	1.28	1.34	2.22	Z = NOT((A1+A2)*B1*B2)
ON4221	6-38	1	2	0.40	0.66	0.35	0.58	1.44	2.39	0.72	1.20	Z = NOT((A1+A2)*(B1+B2))
ON5121	6-39	1	3	0.42	0.70	0.48	0.80	0.78	1.29	1.01	1.68	Z = NOT((A1+A2+A3+A4)*B1)
ON5231	6-40	1	3	0.45	0.75	0.52	0.86	0.79	1.31	1.13	1.88	Z = NOT((A1+A2)*(B1+B2)*C1)
ON6221	6-41	1	3	0.78	1.29	0.37	0.61	2.14	3.55	0.68	1.13	Z = NOT((A1+A2+A3)*(B1+B2+B3))
ON6331	6-42	1	3	0.45	0.75	0.41	0.68	1.44	2.39	0.91	1.51	Z = NOT((A1+A2)*(B1+B2)*(C1+C2))
ON8221	6-43	1	4	1.35	2.24	0.39	0.65	2.83	4.70	0.67	1.11	Z = NOT((A1+A2+A3+A4)*(B1+B2+B3+B4))
ON8441	6-44	1	4	0.48	0.80	0.47	0.78	1.44	2.39	1.09	1.81	Z = NOT((A1+A2)*(B1+B2)*(C1+C2)*(D1+D2))
DFNB1	7-1	1	9	1.70	2.82	1.65	2.74	0.75	1.24	0.55	0.91	D Flip-Flop - Negative edge triggered with preset and clear
DFNB2	7-3	2	10	1.86	3.09	1.80	2.99	0.37	0.61	0.31	0.51	D Flip-Flop - Negative edge triggered with preset and clear
DFNC1	7-5	1	8	1.62	2.69	1.56	2.59	0.74	1.23	0.58	0.96	D Flip-Flop - Negative edge triggered with clear only
DFNC2	7-7	2	9	1.72	2.86	1.73	2.87	0.41	0.68	0.32	0.53	D Flip-Flop - Negative edge triggered with clear only

Name	Page	Drive	Cells	Timing Information								Description
				tPLH (ns)		tPHL (ns)		ΔtPLH (ns/pF)		ΔtPHL (ns/pF)		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
DFNN1	7-9	1	7	1.42	2.36	1.37	2.27	0.75	1.24	0.57	0.95	D Flip-Flop - Negative edge triggered
DFNN2	7-10	2	8	1.62	2.69	1.54	2.56	0.34	0.56	0.32	0.53	D Flip-Flop - Negative edge triggered
DFNP1	7-11	1	8	1.27	2.11	1.37	2.27	0.75	1.24	0.57	0.95	D Flip-Flop - Negative edge triggered with preset only
DFNP2	7-13	2	9	1.33	2.21	1.46	2.42	0.40	0.66	0.30	0.50	D Flip-Flop - Negative edge triggered with preset only
DFFB1	7-15	1	9	1.62	2.69	1.70	2.82	0.74	1.23	0.55	0.91	D Flip-Flop - Positive edge triggered with preset and clear
DFFB2	7-17	2	10	1.84	3.05	1.95	3.24	0.38	0.63	0.28	0.46	D Flip-Flop - Positive edge triggered with preset and clear
DFPC1	7-19	1	8	1.56	2.59	1.70	2.82	0.74	1.23	0.57	0.95	D Flip-Flop - Positive edge triggered with clear only
DFPC2	7-21	2	9	1.74	2.89	1.83	3.04	0.38	0.63	0.31	0.51	D Flip-Flop - Positive edge triggered with clear only
DFPN1	7-23	1	7	1.36	2.26	1.46	2.42	0.75	1.24	0.57	0.95	D Flip-Flop - Positive edge triggered
DFPN2	7-24	2	8	1.59	2.64	1.64	2.72	0.37	0.61	0.31	0.51	D Flip-Flop - Positive edge triggered
DFPP1	7-25	1	8	1.21	2.01	1.52	2.52	0.75	1.24	0.57	0.95	D Flip-Flop - Positive edge triggered with preset only
DFPP2	7-27	2	9	1.26	2.09	1.61	2.67	0.40	0.66	0.29	0.48	D Flip-Flop - Positive edge triggered with preset only
JKNB1	7-29	1	11	1.42	2.36	1.42	2.36	0.82	1.36	0.72	1.20	JK Flip-Flop - Negative edge triggered with preset and clear
JKNB2	7-31	2	12	1.49	2.47	1.46	2.42	0.45	0.75	0.38	0.63	JK Flip-Flop - Negative edge triggered with preset and clear
JKNC1	7-33	1	10	1.38	2.29	1.36	2.26	0.82	1.36	0.76	1.26	JK Flip-Flop - Negative edge triggered with clear only
JKNC2	7-35	2	11	1.46	2.42	1.38	2.29	0.45	0.75	0.44	0.73	JK Flip-Flop - Negative edge triggered with clear only
JKNN1	7-37	1	9	1.07	1.78	1.17	1.94	0.75	1.24	0.67	1.11	JK Flip-Flop - Negative edge triggered
JKNN2	7-38	2	10	1.13	1.88	1.14	1.89	0.40	0.66	0.43	0.71	JK Flip-Flop - Negative edge triggered
JKNP1	7-39	1	10	1.19	1.98	1.36	2.26	0.77	1.28	0.74	1.23	JK Flip-Flop - Negative edge triggered with preset only
JKNP2	7-41	2	11	1.26	2.09	1.33	2.21	0.42	0.70	0.47	0.78	JK Flip-Flop - Negative edge triggered with preset only
JKPB1	7-43	1	11	1.47	2.44	1.36	2.26	0.83	1.38	0.74	1.23	JK Flip-Flop - Positive edge triggered with preset and clear
JKPB2	7-45	2	12	1.53	2.54	1.32	2.19	0.46	0.76	0.49	0.81	JK Flip-Flop - Positive edge triggered with preset and clear
JKPC1	7-47	1	10	1.42	2.36	1.30	2.16	0.84	1.39	0.76	1.26	JK Flip-Flop - Positive edge triggered with clear only
JKPC2	7-49	2	11	1.46	2.42	1.30	2.16	0.48	0.80	0.46	0.76	JK Flip-Flop - Positive edge triggered with clear only
JKPN1	7-51	1	9	1.07	1.78	1.19	1.98	0.76	1.26	0.67	1.11	JK Flip-Flop - Positive edge triggered
JKPN2	7-52	2	10	1.17	1.94	1.24	2.06	0.40	0.66	0.37	0.61	JK Flip-Flop - Positive edge triggered
JKPP1	7-53	1	10	1.25	2.07	1.33	2.21	0.78	1.29	0.74	1.23	JK Flip-Flop - Positive edge triggered with preset only
JKPP2	7-55	2	11	1.32	2.19	1.33	2.21	0.41	0.68	0.47	0.78	JK Flip-Flop - Positive edge triggered with preset only
SCNB1	7-57	1	11	1.61	2.67	1.74	2.89	0.74	1.23	0.57	0.95	Scan Flip-Flop - Negative edge triggered with preset and clear
SCNC1	7-59	1	10	1.73	2.87	1.47	2.44	0.74	1.23	0.59	0.98	Scan Flip-Flop - Negative edge triggered with clear only
SCNN1	7-61	1	9	1.36	2.26	1.46	2.42	0.74	1.23	0.57	0.95	Scan Flip-Flop - Negative edge triggered
SCNP1	7-62	1	10	1.37	2.27	1.53	2.54	0.74	1.23	0.57	0.95	Scan Flip-Flop - Negative edge triggered with preset only
SCPB1	7-64	1	11	1.56	2.59	1.84	3.05	0.75	1.24	0.59	0.98	Scan Flip-Flop - Positive edge triggered with preset and clear
SCPC1	7-66	1	10	1.60	2.66	1.73	2.87	0.75	1.24	0.58	0.96	Scan Flip-Flop - Positive edge triggered with clear only
SCPNI	7-68	1	9	1.30	2.16	1.49	2.47	0.74	1.23	0.59	0.98	Scan Flip-Flop - Positive edge triggered
SCPP1	7-69	1	10	1.35	2.24	1.62	2.69	0.73	1.21	0.59	0.98	Scan Flip-Flop - Positive edge triggered with preset only
TFPB1	7-71	1	9	1.82	3.02	1.85	3.07	0.74	1.23	0.60	1.00	T Flip-Flop - Positive edge triggered with preset and clear
TFPB2	7-73	2	10	2.02	3.35	2.04	3.39	0.41	0.68	0.34	0.56	T Flip-Flop - Positive edge triggered with preset and clear
TFPC1	7-75	1	8	1.73	2.87	1.82	3.02	0.81	1.34	0.60	1.00	T Flip-Flop - Positive edge triggered with clear only
TFPC2	7-77	2	9	1.83	3.04	1.94	3.22	0.41	0.68	0.38	0.63	T Flip-Flop - Positive edge triggered with clear only
TFPP1	7-79	1	8	1.33	2.21	1.67	2.77	0.75	1.24	0.60	1.00	T Flip-Flop - Positive edge triggered with preset only
TFPP2	7-81	2	9	1.38	2.29	1.66	2.76	0.38	0.63	0.37	0.61	T Flip-Flop - Positive edge triggered with preset only
LABB1	8-1	1	5	0.63	1.04	0.54	0.90	0.72	1.20	0.57	0.96	Latch - No Buffered clock with preset and clear
LANB1	8-3	1	6	0.77	1.28	0.62	1.03	0.77	1.28	0.58	0.96	Latch - Negative gate with preset and clear
LANB2	8-5	2	7	1.02	1.69	0.75	1.24	0.33	0.55	0.30	0.50	Latch - Negative gate with preset and clear
LANC1	8-7	1	5	0.76	1.26	0.61	1.01	0.77	1.28	0.58	0.96	Latch - Negative gate with clear only
LANC2	8-9	2	6	0.96	1.59	0.67	1.11	0.35	0.58	0.32	0.53	Latch - Negative gate with clear only
LANN1	8-11	1	4	1.06	1.76	1.16	1.93	0.73	1.21	0.55	0.91	Latch - Negative gate
LANN2	8-13	2	5	1.27	2.11	1.29	2.14	0.38	0.63	0.32	0.53	Latch - Negative gate

Name	Page	Drive	Cells	Timing Information								Description
				tPLH (ns)		tPHL (ns)		ΔtPLH (ns/pF)		ΔtPHL (ns/pF)		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
LANP1	8-15	1	5	0.56	0.93	0.53	0.88	0.81	1.34	0.61	1.01	Latch - Negative gate with preset only
LANP2	8-17	2	6	0.78	1.29	0.60	1.00	0.41	0.68	0.34	0.56	Latch - Negative gate with preset only
LAPB1	8-19	1	6	0.83	1.38	0.72	1.20	0.74	1.23	0.60	1.00	Latch - Positive gate with preset and clear
LAPB2	8-21	2	7	0.95	1.58	0.72	1.20	0.40	0.66	0.40	0.66	Latch - Positive gate with preset and clear
LAPC1	8-23	1	5	0.81	1.34	0.70	1.16	0.74	1.23	0.61	1.01	Latch - Positive gate with clear only
LAPC2	8-25	2	6	0.96	1.59	0.72	1.20	0.41	0.68	0.40	0.66	Latch - Positive gate with clear only
LAPN1	8-27	1	4	1.06	1.76	1.08	1.79	0.73	1.21	0.57	0.95	Latch - Positive gate
LAPN2	8-29	2	5	1.27	2.11	1.24	2.06	0.40	0.66	0.36	0.60	Latch - Positive gate
LAPP1	8-31	1	5	0.72	1.20	0.53	0.88	0.74	1.23	0.58	0.96	Latch - Positive gate with preset only
LAPP2	8-33	2	6	0.93	1.54	0.59	0.98	0.34	0.56	0.32	0.53	Latch - Positive gate with preset only
LTPB1	8-35	1	13	0.82	1.36	0.75	1.24	0.75	1.24	0.61	1.01	Latch with Tri-state - Positive gate with preset and clear
LTPC1	8-38	1	12	0.82	1.36	0.75	1.24	0.75	1.24	0.61	1.01	Latch with Tri-state - Positive gate with clear only
LTPN1	8-41	1	11	0.82	1.36	0.75	1.24	0.75	1.24	0.61	1.01	Latch with Tri-state - Positive gate
LTPP1	8-44	1	12	0.82	1.36	0.75	1.24	0.75	1.24	0.61	1.01	Latch with Tri-state - Positive gate with preset only
MXH211	9-1	1	4	0.08	0.13	0.19	0.32	0.73	1.21	0.97	1.61	2 to 1 multiplexer active high gated output
MXH411	9-2	1	9	0.18	0.30	0.18	0.30	0.72	1.20	0.98	1.63	4 to 1 multiplexer active high gated output
MXL211	9-3	1	4	0.05	0.08	0.18	0.30	1.61	2.67	0.57	0.95	2 to 1 multiplexer active low gated output
MXL411	9-4	1	9	0.07	0.12	0.18	0.30	1.58	2.62	0.57	0.95	4 to 1 multiplexer active low gated output
MXN211	9-5	1	3	0.58	0.96	0.64	1.06	0.74	1.23	0.66	1.10	2 to 1 multiplexer
MXN411	9-6	1	8	1.32	2.19	1.90	3.15	1.10	1.83	0.93	1.54	4 to 1 multiplexer
MIH211	9-7	1	4	0.08	0.13	0.19	0.32	0.73	1.21	0.97	1.61	2 to 1 inverting multiplexer active high gated output
MIH411	9-8	1	8	0.18	0.30	0.16	0.27	0.72	1.20	0.99	1.64	4 to 1 inverting multiplexer active high gated output
MIL211	9-9	1	4	0.07	0.12	0.16	0.27	1.58	2.62	0.57	0.95	2 to 1 inverting multiplexer active low gated output
MIL411	9-10	1	8	0.08	0.13	0.18	0.30	1.58	2.62	0.57	0.95	4 to 1 inverting multiplexer active low gated output
MIN211	9-11	1	4	0.22	0.37	0.41	0.68	1.45	2.41	0.98	1.63	2 to 1 inverting multiplexer
MIN411	9-12	1	8	1.14	1.89	1.25	2.07	0.74	1.23	0.62	1.03	4 to 1 inverting multiplexer
DEH241	9-13	1	8	0.78	1.29	0.73	1.21	2.17	3.60	0.58	0.96	2 to 4 active high outputs decoder active High gated output
DEL241	9-14	1	8	0.89	1.48	1.02	1.69	2.13	3.54	0.59	0.98	2 to 4 active high outputs decoder active low gated output
DEN241	9-15	1	5	0.26	0.43	0.25	0.41	1.41	2.34	0.58	0.96	2 to 4 active high outputs decoder
DIH241	9-16	1	8	0.72	1.20	0.75	1.21	0.75	1.24	1.31	2.17	2 to 4 active low outputs decoder active high gated output
DIL241	9-17	1	8	0.56	0.93	0.85	1.41	0.76	1.26	1.30	2.16	2 to 4 active low outputs decoder active Low gated output
DIN241	9-18	1	5	0.53	0.88	0.47	0.78	0.76	1.26	0.93	1.54	2 to 4 active low outputs decoder
CDQY4	10-1	-	-	12.12	3.52	2.10	3.49	ps/pF	ps/pF	ps/pF	ps/pF	Z = A. Implementation is using an inverter tree to allow high drive of clock nets while minimizing skew
HILO	10-2	-	2									The HILO internal tie off gate is offered for managing unused inputs
BUSHOLD	10-3	-	2									Retains the value of an undriven bus
IPN	11-1	-	pad									Input pad
IPD	11-2	-	pad									Input pad with pull-down
IPU	11-3	-	pad									Input pad with pull-up
IPCBC1	11-4	1	2	0.40	0.66	0.26	0.43	0.74	1.23	0.55	0.91	CMOS level shifter
IPCBC2	11-5	2	2	0.47	0.78	0.34	0.56	0.37	0.61	0.28	0.46	CMOS level shifter
IPCBC4	11-6	4	4	0.43	0.71	0.37	0.61	0.19	0.32	0.15	0.25	CMOS level shifter
IPCBC8	11-7	8	6	0.58	0.96	0.53	0.88	0.09	0.15	0.07	0.12	CMOS level shifter
IPCIC1	11-8	1	2	0.40	0.66	0.65	1.08	0.75	1.24	0.55	0.91	Inverting CMOS level shifter
IPCIC2	11-9	2	3	0.47	0.78	0.73	1.21	0.37	0.61	0.30	0.50	Inverting CMOS level shifter
IPCIC4	11-10	4	4	0.55	0.91	0.78	1.29	0.19	0.32	0.16	0.27	Inverting CMOS level shifter
IPCIC8	11-11	8	6	0.66	1.10	1.00	1.66	0.09	0.15	0.08	0.13	Inverting CMOS level shifter
IPHBC1	11-12	1	5	0.69	1.15	0.72	1.20	0.74	1.23	0.57	0.95	CMOS level shifter with hysteresis

Name	Page	Drive	Cells	Timing Information								Description
				tPLH (ns)		tPHL (ns)		ΔtPLH (ns/pF)		ΔtPHL (ns/pF)		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
IPHBC2	11-13	2	5	0.73	1.21	0.77	1.28	0.38	0.63	0.32	0.53	CMOS level shifter with hysteresis
IPHBC4	11-14	4	6	0.82	1.36	0.89	1.48	0.21	0.35	0.20	0.33	CMOS level shifter with hysteresis
IPHBC8	11-15	8	8	1.06	1.76	1.25	2.07	0.10	0.17	0.09	0.15	CMOS level shifter with hysteresis
IPHIC1	11-16	1	5	0.83	1.38	0.95	1.58	0.75	1.24	0.55	0.91	Inverting CMOS level shifter with hysteresis
IPHIC2	11-17	2	6	0.94	1.56	1.05	1.74	0.37	0.61	0.30	0.50	Inverting CMOS level shifter with hysteresis
IPHIC4	11-18	4	7	1.01	1.68	1.07	1.78	0.19	0.32	0.16	0.27	Inverting CMOS level shifter with hysteresis
IPHIC8	11-19	8	9	1.17	1.94	1.32	2.19	0.09	0.15	0.08	0.13	Inverting CMOS level shifter with hysteresis
IPSBC1	11-20	1	5	0.43	0.71	1.47	2.44	0.74	1.23	0.95	1.58	TTL level shifter with hysteresis
IPSBC2	11-21	2	5	0.47	0.78	1.67	2.77	0.37	0.61	0.54	0.90	TTL level shifter with hysteresis
IPSBC4	11-22	4	6	0.56	0.93	2.10	3.49	0.20	0.33	0.35	0.58	TTL level shifter with hysteresis
IPSBC8	11-23	8	10	1.14	1.89	2.13	3.54	0.09	0.15	0.11	0.18	TTL level shifter with hysteresis
IPSIC1	11-24	1	5	1.46	2.42	0.72	1.20	0.74	1.23	0.88	1.46	Inverting TTL level shifter with hysteresis
IPSIC2	11-25	2	6	1.56	2.59	0.83	1.38	0.37	0.61	0.44	0.73	Inverting TTL level shifter with hysteresis
IPSIC4	11-26	4	7	1.82	3.02	0.85	1.41	0.19	0.32	0.24	0.40	Inverting TTL level shifter with hysteresis
IPSIC8	11-27	8	9	2.02	3.35	1.08	1.79	0.09	0.15	0.11	0.18	Inverting TTL level shifter with hysteresis
IPTBC1	11-28	1	2	0.26	0.43	0.69	1.15	0.75	1.24	0.90	1.49	TTL level shifter
IPTBC2	11-29	2	2	0.31	0.51	0.83	1.38	0.37	0.61	0.50	0.83	TTL level shifter
IPTBC4	11-30	4	3	0.39	0.65	1.16	1.93	0.19	0.32	0.31	0.51	TTL level shifter
IPTIC1	11-31	1	2	0.72	1.20	0.56	0.93	0.74	1.23	0.85	1.41	Inverting TTL level shifter
IPTIC2	11-32	2	3	0.78	1.29	0.66	1.10	0.38	0.63	0.43	0.71	Inverting TTL level shifter
IPTIC4	11-33	4	4	0.96	1.59	0.69	1.15	0.20	0.33	0.23	0.38	Inverting TTL level shifter
IPTIC8	11-34	8	6	1.13	1.88	0.93	1.54	0.09	0.15	0.12	0.20	Inverting TTL level shifter
VDDPAD	14-1	-	pad									VDD power pad supplies power (VDD) to the core of the array
VCCPAD	14-2	-	pad									VCC power pad supplies power (VDD) to the external I/Os
VSSPAD	14-3	-	pad									VSS power pad supplies ground to the core of the array
GNDPAD	14-4	-	pad									GND power pad supplies ground to the external I/Os
CNCT_PWR	14-5	-	none									Connects the VDD core bus with the VCC I/O bus
CNCT_GRND	14-6	-	none									Connects the VSS core bus with the GND I/O bus
COCIN	14-7	-	pad									Input part of crystal oscillator
COCO1	14-8	1	pad	2.53	4.22	1.82	3.05	0.21	0.34	0.13	0.23	Output part of crystal oscillator
COCO2	14-9	2	pad	1.27	2.13	0.99	1.65	0.10	0.18	0.07	0.11	Output part of crystal oscillator
COCO4	14-10	4	pad	0.66	1.12	0.58	0.96	0.05	0.09	0.03	0.07	Output part of crystal oscillator

Name	Page	Output Drive	Timing Information (CL = 100pF)								Description
			tPLH (ns)		tPHL (ns)		ΔtPLH (ps/pF)		ΔtPHL (ps/pF)		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
OSST02	12-1	2 mA	25.1	41.7	28.3	47.1	205	341	217	360	TTL level tri-state with slew-rate
OSST04	12-3	4 mA	13.9	23.1	16.5	27.4	103	170	109	180	TTL level tri-state with slew-rate
OSST06	12-5	6 mA	10.3	17.2	12.7	21.1	68	114	74	123	TTL level tri-state with slew-rate
OSST08	12-7	8 mA	8.73	14.4	11.0	18.3	51	85	57	94	TTL level tri-state with slew-rate
OSST12	12-9	12 mA	6.49	10.7	8.31	13.7	33	55	40	66	TTL level tri-state with slew-rate
OSST16	12-11	16 mA	5.63	9.35	7.17	11.9	25	42	32	53	TTL level tri-state with slew-rate
OSSC02	12-13	2 mA	32.2	53.4	22.5	37.4	267	444	166	276	CMOS level tri-state with slew-rate
OSSC04	12-15	4 mA	17.6	29.2	13.6	22.6	133	221	83	138	CMOS level tri-state with slew-rate
OSSC06	12-17	6 mA	13.0	21.6	10.9	18.1	89	148	57	94	CMOS level tri-state with slew-rate
OSSC08	12-19	8 mA	10.6	17.6	9.79	16.2	65	107	44	73	CMOS level tri-state with slew-rate
OSSC12	12-21	12 mA	8.04	13.3	7.41	12.3	42	70	31	52	CMOS level tri-state with slew-rate
OSSC16	12-23	16 mA	7.10	11.7	6.45	10.7	33	54	26	42	CMOS level tri-state with slew-rate
OSTT02	12-25	2 mA	24.7	41.0	27.4	45.6	205	341	217	360	TTL level totem-pole with slew-rate
OSTT04	12-26	4 mA	13.4	22.3	15.5	25.8	103	170	108	180	TTL level totem-pole with slew-rate
OSTT06	12-27	6 mA	9.86	16.3	11.7	19.5	68	114	74	122	TTL level totem-pole with slew-rate
OSTT08	12-28	8 mA	8.16	13.5	9.95	16.5	51	85	56	93	TTL level totem-pole with slew-rate
OSTT12	12-29	12 mA	6.28	10.4	7.91	13.1	33	55	40	66	TTL level totem-pole with slew-rate
OSTT16	12-30	16 mA	5.51	9.14	6.95	11.5	25	42	32	53	TTL level totem-pole with slew-rate
OSTC02	12-31	2 mA	31.7	52.7	21.6	35.9	267	444	166	275	CMOS level totem-pole with slew-rate
OSTC04	12-32	4 mA	17.0	28.3	12.6	21.0	133	221	83	138	CMOS level totem-pole with slew-rate
OSTC06	12-33	6 mA	12.4	20.7	9.82	16.3	89	148	56	93	CMOS level totem-pole with slew-rate
OSTC08	12-34	8 mA	10.0	16.6	8.53	14.1	65	107	43	72	CMOS level totem-pole with slew-rate
OSTC12	12-35	12 mA	7.80	12.9	6.95	11.5	42	70	31	52	CMOS level totem-pole with slew-rate
OSTC16	12-36	16 mA	6.97	11.5	6.20	10.2	32	54	25	42	CMOS level totem-pole with slew-rate
OSDT02	12-37	2 mA	25.2	41.8	28.2	46.9	206	341	216	358	TTL level tri-state with pull-down and slew-rate
OSDT04	12-39	4 mA	13.9	23.1	16.4	27.3	103	171			TTL level tri-state with pull-down and slew-rate
OSDT06	12-41	6 mA	10.4	17.2	12.7	21.1	68	114	74	123	TTL level tri-state with pull-down and slew-rate
OSDT08	12-43	8 mA	8.74	14.5	11.0	18.3	51	85	57	94	TTL level tri-state with pull-down and slew-rate
OSDT12	12-45	12 mA	6.49	10.7	8.30	13.7	33	55	40	66	TTL level tri-state with pull-down and slew-rate
OSDT16	12-47	16 mA	5.63	9.35	7.17	11.9	25	42	32	53	TTL level tri-state with pull-down and slew-rate
OSDC02	12-49	2 mA	32.3	53.6	22.4	37.2	268	445	165	274	CMOS level tri-state with pull-down and slew-rate
OSDC04	12-51	4 mA	17.6	29.2	13.6	22.6	133	221	83	138	CMOS level tri-state with pull-down and slew-rate
OSDC06	12-53	6 mA	13.0	21.6	10.9	18.1	89	148	56	94	CMOS level tri-state with pull-down and slew-rate
OSDC08	12-55	8 mA	10.6	17.7	9.78	16.2	65	107	44	73	CMOS level tri-state with pull-down and slew-rate
OSDC12	12-57	12 mA	8.04	13.3	7.41	12.3	42	70	31	52	CMOS level tri-state with pull-down and slew-rate
OSDC16	12-59	16 mA	7.10	11.7	6.45	10.7	33	54	26	42	CMOS level tri-state with pull-down and slew-rate
OSNT02	12-61	2 mA			27.5	45.7			220	365	TTL level N-channel open drain with slew-rate
OSNT04	12-62	4 mA			15.4	25.6			110	182	TTL level N-channel open drain with slew-rate
OSNT06	12-63	6 mA			11.5	19.1			74	122	TTL level N-channel open drain with slew-rate
OSNT08	12-64	8 mA			9.66	16.0			56	93	TTL level N-channel open drain with slew-rate
OSNT12	12-65	12 mA			7.63	12.6			40	66	TTL level N-channel open drain with slew-rate
OSNT16	12-66	16 mA			6.68	11.0			32	53	TTL level N-channel open drain with slew-rate
OSNC02	12-67	2 mA			21.5	35.7			166	276	CMOS level N-channel open drain with slew-rate
OSNC04	12-68	4 mA			12.4	20.6			83	138	CMOS level N-channel open drain with slew-rate
OSNC06	12-69	6 mA			9.49	15.7			56	93	CMOS level N-channel open drain with slew-rate
OSNC08	12-70	8 mA			8.09	13.4			43	72	CMOS level N-channel open drain with slew-rate
OSNC12	12-71	12 mA			6.51	10.8			31	51	CMOS level N-channel open drain with slew-rate
OSNC16	12-72	16 mA			5.78	9.60			25	42	CMOS level N-channel open drain with slew-rate
OSOT02	12-73	2 mA			27.5	45.7			220	365	TTL level N-channel open drain with pull-up and slew-rate

Name	Page	Output Drive	Timing Information (CL = 100pF)								Description
			tPLH (ns)		tPHL (ns)		ΔtPLH (ps/pF)		ΔtPHL (ps/pF)		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
OSOT04	12-74	4 mA			15.4	25.6			110	182	TTL level N-channel open drain with pull-up and slew-rate
OSOT06	12-75	6 mA			11.5	19.1			74	122	TTL level N-channel open drain with pull-up and slew-rate
OSOT08	12-76	8 mA			9.67	16.0			56	93	TTL level N-channel open drain with pull-up and slew-rate
OSOT12	12-77	12 mA			7.63	12.6			40	66	TTL level N-channel open drain with pull-up and slew-rate
OSOT16	12-78	16 mA			6.68	11.0			32	53	TTL level N-channel open drain with pull-up and slew-rate
OSOC02	12-79	2 mA			21.5	35.7			166	276	CMOS level N-channel open drain with pull-up and slew-rate
OSOC04	12-80	4 mA			12.4	20.6			83	138	CMOS level N-channel open drain with pull-up and slew-rate
OSOC06	12-81	6 mA			9.49	15.7			56	93	CMOS level N-channel open drain with pull-up and slew-rate
OSOC08	12-82	8 mA			8.10	13.4			43	72	CMOS level N-channel open drain with pull-up and slew-rate
OSOC12	12-83	12 mA			6.52	10.8			31	51	CMOS level N-channel open drain with pull-up and slew-rate
OSOC16	12-84	16 mA			5.78	9.60			25	42	CMOS level N-channel open drain with pull-up and slew-rate
OSPT02	12-85	2 mA	24.6	40.9			205	341			TTL level P-channel open drain with slew-rate
OSPT04	12-86	4 mA	13.3	22.2			103	170			TTL level P-channel open drain with slew-rate
OSPT06	12-87	6 mA	9.72	16.1			68	114			TTL level P-channel open drain with slew-rate
OSPT08	12-88	8 mA	7.97	13.2			51	85			TTL level P-channel open drain with slew-rate
OSPT12	12-89	12 mA	6.08	10.0			33	55			TTL level P-channel open drain with slew-rate
OSPT16	12-90	16 mA	5.31	8.81			25	42			TTL level P-channel open drain with slew-rate
OSPC02	12-91	2 mA	31.7	52.6			267	444			CMOS level P-channel open drain with slew-rate
OSPC04	12-92	4 mA	17.0	28.2			133	221			CMOS level P-channel open drain with slew-rate
OSPC06	12-93	6 mA	12.3	20.4			89	148			CMOS level P-channel open drain with slew-rate
OSPC08	12-94	8 mA	9.85	16.3			65	107			CMOS level P-channel open drain with slew-rate
OSPC12	12-95	12 mA	7.61	12.6			42	70			CMOS level P-channel open drain with slew-rate
OSPC16	12-96	16 mA	6.77	11.2			32	54			CMOS level P-channel open drain with slew-rate
OSQT02	12-97	2 mA	24.7	41.0			206	341			TTL level P-channel open drain with pull-down and slew-rate
OSQT04	12-98	4 mA	13.4	22.2			103	170			TTL level P-channel open drain with pull-down and slew-rate
OSQT06	12-99	6 mA	9.73	16.1			68	114			TTL level P-channel open drain with pull-down and slew-rate
OSQT08	12-100	8 mA	7.97	13.2			51	85			TTL level P-channel open drain with pull-down and slew-rate
OSQT12	12-101	12 mA	6.09	10.1			33	55			TTL level P-channel open drain with pull-down and slew-rate
OSQT16	12-102	16 mA	5.31	8.81			25	42			TTL level P-channel open drain with pull-down and slew-rate
OSQC02	12-103	2 mA	31.8	52.7			268	445			CMOS level P-channel open drain with pull-down and slew-rate
OSQC04	12-104	4 mA	17.0	28.2			133	221			CMOS level P-channel open drain with pull-down and slew-rate
OSQC06	12-105	6 mA	12.3	20.5			89	148			CMOS level P-channel open drain with pull-down and slew-rate
OSQC08	12-106	8 mA	9.86	16.3			65	107			CMOS level P-channel open drain with pull-down and slew-rate
OSQC12	12-107	12 mA	7.61	12.6							CMOS level P-channel open drain with pull-down and slew-rate

Name	Page	Output Drive	Timing Information (CL = 100pF)								Description
			tPLH (ns)		tPHL (ns)		ΔtPLH (ps/pF)		ΔtPHL (ps/pF)		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
OSQC16	12-108	16 mA	6.77	11.2			32	54			CMOS level P-channel open drain with pull-down and slew-rate
OSUT02	12-109	2 mA	25.0	41.5	28.4	47.1	204	339	217	360	TTL level tri-state with pull-up and slew-rate
OSUT04	12-111	4 mA	13.9	23.1	16.5	27.4	102	170	109	181	TTL level tri-state with pull-up and slew-rate
OSUT06	12-113	6 mA	10.3	17.2	12.7	21.2	68	113	74	123	TTL level tri-state with pull-up and slew-rate
OSUT08	12-115	8 mA	8.72	14.4	11.0	18.3	51	85	57	94	TTL level tri-state with pull-up and slew-rate
OSUT12	12-117	12 mA	6.49	10.7	8.31	13.7	33	55	40	66	TTL level tri-state with pull-up and slew-rate
OSUT16	12-119	16 mA	5.63	9.35	7.17	11.9	25	42	32	53	TTL level tri-state with pull-up and slew-rate
OSUC02	12-121	2 mA	32.1	53.3	22.5	37.4	266	442	166	276	CMOS level tri-state with pull-up and slew-rate
OSUC04	12-123	4 mA	17.5	29.1	13.6	22.7	133	220	83	138	CMOS level tri-state with pull-up and slew-rate
OSUC06	12-125	6 mA	13.0	21.6	10.9	18.2	89	147	57	94	CMOS level tri-state with pull-up and slew-rate
OSUC08	12-127	8 mA	10.6	17.6	9.79	16.2	65	107	44	73	CMOS level tri-state with pull-up and slew-rate
OSUC12	12-129	12 mA	8.03	13.3	7.41	12.3	42	70	31	52	CMOS level tri-state with pull-up and slew-rate
OSUC16	12-131	16 mA	7.09	11.7	6.45	10.7	33	54	26	42	CMOS level tri-state with pull-up and slew-rate
OMST12	12-133	12 mA	5.49	9.11	6.99	11.6	33	55	38	62	TTL level tri-state with moderate slew-rate
OMST16	12-135	16 mA	4.47	7.43	5.76	9.57	24	41	29	48	TTL level tri-state with moderate slew-rate
OMSC12	12-137	12 mA	6.75	11.2	6.20	10.3	42	69	29	48	CMOS level tri-state with moderate slew-rate
OMSC16	12-139	16 mA	5.61	9.32	5.15	8.56	31	52	22	37	CMOS level tri-state with moderate slew-rate
OMTT12	12-141	12 mA	5.25	8.71	6.52	10.8	33	55	37	62	TTL level totem-pole with moderate slew-rate
OMTT16	12-142	16 mA	4.09	6.79	5.05	8.38	24	41	28	47	TTL level totem-pole with moderate slew-rate
OMTC12	12-143	12 mA	6.48	10.7	5.64	9.36	42	69	29	47	CMOS level totem-pole with moderate slew-rate
OMTC16	12-144	16 mA	5.14	8.53	4.42	7.34	31	52	22	36	CMOS level totem-pole with moderate slew-rate
OMDT12	12-145	12 mA	5.49	9.11	6.99	11.6	33	55	37	62	TTL level tri-state with pull-down and moderate slew-rate
OMDT16	12-147	16 mA	4.47	7.43	5.76	9.57	24	41	29	48	TTL level tri-state with pull-down and moderate slew-rate
OMDC12	12-149	12 mA	6.75	11.2	6.20	10.3	42	69	29	48	CMOS level tri-state with pull-down and moderate slew-rate
OMDC16	12-151	16 mA	5.61	9.32	5.15	8.56	31	52	22	37	CMOS level tri-state with pull-down and moderate slew-rate
OMNT12	12-153	12 mA			6.24	10.3			37	62	TTL level N-channel open drain with moderate slew-rate
OMNT16	12-154	16 mA			4.77	7.91			28	47	TTL level N-channel open drain with moderate slew-rate
OMNC12	12-155	12 mA			5.20	8.63			28	47	CMOS level N-channel open drain with moderate slew-rate
OMNC16	12-156	16 mA			3.97	6.60			22	36	CMOS level N-channel open drain with moderate slew-rate
OMOT12	12-157	12 mA			6.24	10.3			37	62	TTL level N-channel open drain with pull-up and moderate slew-rate
OMOT16	12-158	16 mA			4.77	7.91			28	47	TTL level N-channel open drain with pull-up and moderate slew-rate
OMOC12	12-159	12 mA			5.20	8.63			28	47	CMOS level N-channel open drain with pull-up and moderate slew-rate
OMOC16	12-160	16 mA			3.97	6.60			22	36	CMOS level N-channel open drain with pull-up and moderate slew-rate
OMPT12	12-161	12 mA	5.06	8.40			33	55			TTL level P-channel open drain with moderate slew-rate
OMPT16	12-162	16 mA	3.90	6.47			24	41			TTL level P-channel open drain with moderate slew-rate
OMPC12	12-163	12 mA	6.31	10.4			42	69			CMOS level P-channel open drain with moderate slew-rate
OMPC16	12-164	16 mA	4.95	8.22			31	52			CMOS level P-channel open drain with moderate slew-rate
OMQT12	12-165	12 mA	5.06	8.40			33	55			TTL level P-channel open drain with pull-down and moderate slew-rate
OMQT16	12-166	16 mA	3.91	6.48			24	41			TTL level P-channel open drain with pull-down and moderate slew-rate
OMQC12	12-167	12 mA	6.31	10.4			42	69			CMOS level P-channel open drain with pull-down and moderate slew-rate

Name	Page	Output Drive	Timing Information (CL = 100pF)								Description
			tPLH (ns)		tPHL (ns)		ΔtPLH (ps/pF)		ΔtPHL (ps/pF)		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
OMQC16	12-168	16 mA	4.95	8.22			31	52			CMOS level P-channel open drain with pull-down and moderate slew-rate
OMUT12	12-169	12 mA	5.48	9.09	6.99	11.6	33	55	38	62	TTL level tri-state with pull-up and moderate slew-rate
OMUT16	12-171	16 mA	4.47	7.43	5.76	9.57	24	41	29	48	TTL level tri-state with pull-up and moderate slew-rate
OMUC12	12-173	12 mA	6.75	11.2	6.20	10.3	42	69	29	48	CMOS level tri-state with pull-up and moderate slew-rate
OMUC16	12-175	16 mA	5.61	9.32	5.15	8.56	31	52	23	37	CMOS level tri-state with pull-up and moderate slew-rate
ONST02	12-177	2 mA	23.9	39.7	26.1	43.4	205	341	217	360	TTL level tri-state
ONST04	12-179	4 mA	12.6	20.9	14.1	23.4	103	170	108	180	TTL level tri-state
ONST06	12-181	6 mA	8.40	13.9	9.38	15.5	68	114	73	121	TTL level tri-state
ONST08	12-183	8 mA	6.55	10.8	7.46	12.3	51	85	54	90	TTL level tri-state
ONST12	12-185	12 mA	4.43	7.35	5.19	8.61	33	55	36	60	TTL level tri-state
ONST16	12-187	16 mA	3.54	5.88	4.31	7.16	24	41	27	45	TTL level tri-state
ONSC02	12-189	2 mA	30.9	51.3	20.3	33.7	267	444	166	275	CMOS level tri-state
ONSC04	12-191	4 mA	16.0	26.6	11.2	18.6	133	221	83	137	CMOS level tri-state
ONSC06	12-193	6 mA	10.7	17.8	7.48	12.4	89	147	55	91	CMOS level tri-state
ONSC08	12-195	8 mA	8.09	13.4	6.08	10.1	64	107	41	69	CMOS level tri-state
ONSC12	12-197	12 mA	5.47	9.08	4.29	7.13	42	69	28	46	CMOS level tri-state
ONSC16	12-199	16 mA	4.43	7.35	3.69	6.13	31	52	21	34	CMOS level tri-state
ONTT02	12-201	2 mA	23.5	39.0	25.3	42.1	205	341	217	360	TTL level totem-pole
ONTT04	12-202	4 mA	11.8	19.7	12.8	21.2	103	170	108	180	TTL level totem-pole
ONTT06	12-203	6 mA	8.10	13.4	8.79	14.5	68	114	73	121	TTL level totem-pole
ONTT08	12-204	8 mA	6.16	10.2	6.70	11.1	51	85	54	90	TTL level totem-pole
ONTT12	12-205	12 mA	4.13	6.86	4.68	7.78	33	55	36	60	TTL level totem-pole
ONTT16	12-206	16 mA	3.22	5.34	3.77	6.26	24	41	27	45	TTL level totem-pole
ONTC02	12-207	2 mA	30.4	50.5	19.5	32.4	267	444	166	275	CMOS level totem-pole
ONTC04	12-208	4 mA	15.2	25.3	9.91	16.4	133	221	83	137	CMOS level totem-pole
ONTC06	12-209	6 mA	10.4	17.2	6.88	11.4	89	147	55	91	CMOS level totem-pole
ONTC08	12-210	8 mA	7.65	12.6	5.30	8.80	64	107	41	69	CMOS level totem-pole
ONTC12	12-211	12 mA	5.11	8.48	3.79	6.30	42	69	27	46	CMOS level totem-pole
ONTC16	12-212	16 mA	4.01	6.66	3.16	5.24	31	52	21	34	CMOS level totem-pole
ONDT02	12-213	2 mA	24.0	39.8	26.0	43.2	206	341	216	358	TTL level tri-state with pull-down
ONDT04	12-215	4 mA	12.6	20.9	14.0	23.3	103	170	108	179	TTL level tri-state with pull-down
ONDT06	12-217	6 mA	8.42	13.9	9.37	15.5	68	114	73	120	TTL level tri-state with pull-down
ONDT08	12-219	8 mA	6.56	10.9	7.45	12.3	51	85	54	90	TTL level tri-state with pull-down
ONDT12	12-221	12 mA	4.43	7.35	5.19	8.61	33	55			TTL level tri-state with pull-down
ONDT16	12-223	16 mA	3.54	5.88	4.31	7.16	24	41	27	45	TTL level tri-state with pull-down
ONDC02	12-225	2 mA	31.0	51.4	20.2	33.6	268	445	165	274	CMOS level tri-state with pull-down
ONDC04	12-227	4 mA	16.1	26.7	11.2	18.6	133	221	83	137	CMOS level tri-state with pull-down
ONDC06	12-229	6 mA	10.7	17.8	7.47	12.4	89	148	55	91	CMOS level tri-state with pull-down
ONDC08	12-231	8 mA	8.11	13.4	6.08	10.1	64	107	41	68	CMOS level tri-state with pull-down
ONDC12	12-233	12 mA	5.47	9.08	4.29	7.13	42	69	28	46	CMOS level tri-state with pull-down
ONDC16	12-235	16 mA	4.43	7.36	3.69	6.13	31	52	21	34	CMOS level tri-state with pull-down
ONNT02	12-237	2 mA			25.4	42.1			220	365	TTL level N-channel open drain
ONNT04	12-238	4 mA			12.7	21.2			110	182	TTL level N-channel open drain
ONNT06	12-239	6 mA			8.69	14.4			73	121	TTL level N-channel open drain
ONNT08	12-240	8 mA			6.61	10.9			55	91	TTL level N-channel open drain
ONNT12	12-241	12 mA			4.55	7.55			36	60	TTL level N-channel open drain
ONNT16	12-242	16 mA			3.57	5.93			27	45	TTL level N-channel open drain
ONNC02	12-243	2 mA			19.4	32.2			166	276	CMOS level N-channel open drain

Name	Page	Output Drive	Timing Information (CL = 100pF)								Description
			tPLH (ns)		tPHL (ns)		ΔtPLH (ps/pF)		ΔtPHL (ps/pF)		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
ONNC04	12-244	4 mA			9.81	16.2			83	138	CMOS level N-channel open drain
ONNC06	12-245	6 mA			6.71	11.1			55	91	CMOS level N-channel open drain
ONNC08	12-246	8 mA			5.12	8.51			41	68	CMOS level N-channel open drain
ONNC12	12-247	12 mA			3.56	5.91			27	46	CMOS level N-channel open drain
ONNC16	12-248	16 mA			2.83	4.69			21	34	CMOS level N-channel open drain
ONOT02	12-249	2 mA			25.4	42.2					TTL level N-channel open drain with pull-up
ONOT04	12-250	4 mA			12.8	21.2			110	182	TTL level N-channel open drain with pull-up
ONOT06	12-251	6 mA			8.70	14.4			73	121	TTL level N-channel open drain with pull-up
ONOT08	12-252	8 mA			6.61	10.9					TTL level N-channel open drain with pull-up
ONOT12	12-253	12 mA			4.55	7.55			36	60	TTL level N-channel open drain with pull-up
ONOT16	12-254	16 mA			3.57	5.93			27	45	TTL level N-channel open drain with pull-up
ONOC02	12-255	2 mA			19.4	32.3			166	276	CMOS level N-channel open drain with pull-up
ONOC04	12-256	4 mA			9.81	16.2			83	138	CMOS level N-channel open drain with pull-up
ONOC06	12-257	6 mA			6.71	11.1			55	91	CMOS level N-channel open drain with pull-up
ONOC08	12-258	8 mA			5.12	8.51			41	69	CMOS level N-channel open drain with pull-up
ONOC12	12-259	12 mA			3.56	5.91			27	46	CMOS level N-channel open drain with pull-up
ONOC16	12-260	16 mA			2.83	4.69			21	34	CMOS level N-channel open drain with pull-up
ONPT02	12-261	2 mA	23.4	38.9			205	341			TTL level P-channel open drain
ONPT04	12-262	4 mA	11.8	19.6			103	170			TTL level P-channel open drain
ONPT06	12-263	6 mA	8.01	13.2			68	114			TTL level P-channel open drain
ONPT08	12-264	8 mA	6.07	10.0			51	85			TTL level P-channel open drain
ONPT12	12-265	12 mA	4.02	6.68			33	55			TTL level P-channel open drain
ONPT16	12-266	16 mA	3.08	5.11			24	41			TTL level P-channel open drain
ONPC02	12-267	2 mA	30.3	50.4			267	444			CMOS level P-channel open drain
ONPC04	12-268	4 mA	15.2	25.2			133	221			CMOS level P-channel open drain
ONPC06	12-269	6 mA	10.3	17.1			89	147			CMOS level P-channel open drain
ONPC08	12-270	8 mA	7.55	12.5			64	107			CMOS level P-channel open drain
ONPC12	12-271	12 mA	5.01	8.32			42	69			CMOS level P-channel open drain
ONPC16	12-272	16 mA	3.89	6.46			31	52			CMOS level P-channel open drain
ONQT02	12-273	2 mA	23.5	39.0			206	341			TTL level P-channel open drain with pull-down
ONQT04	12-274	4 mA	11.8	19.6			103	170			TTL level P-channel open drain with pull-down
ONQT06	12-275	6 mA	8.01	13.2			68	114			TTL level P-channel open drain with pull-down
ONQT08	12-276	8 mA	6.07	10.0			51	85			TTL level P-channel open drain with pull-down
ONQT12	12-277	12 mA	4.02	6.68			33	55			TTL level P-channel open drain with pull-down
ONQT16	12-278	16 mA	3.08	5.11			24	41			TTL level P-channel open drain with pull-down
ONQC02	12-279	2 mA	30.4	50.5			268	445			CMOS level P-channel open drain with pull-down
ONQC04	12-280	4 mA	15.2	25.3			133	221			CMOS level P-channel open drain with pull-down
ONQC06	12-281	6 mA	10.3	17.1			89	148			CMOS level P-channel open drain with pull-down
ONQC08	12-282	8 mA	7.56	12.5			64	107			CMOS level P-channel open drain with pull-down
ONQC12	12-283	12 mA	5.01	8.32			42	69			CMOS level P-channel open drain with pull-down
ONQC16	12-284	16 mA	3.89	6.46			31	52			CMOS level P-channel open drain with pull-down
ONUT02	12-285	2 mA	23.8	39.5	26.2	43.5	204	339	217	360	TTL level tri-state with pull-up
ONUT04	12-287	4 mA	12.5	20.8	14.1	23.4	102	170	108	180	TTL level tri-state with pull-up
ONUT06	12-289	6 mA	8.39	13.9	9.38	15.5	68	113	73	121	TTL level tri-state with pull-up
ONUT08	12-291	8 mA	6.55	10.8	7.46	12.3	51	85	54	90	TTL level tri-state with pull-up
ONUT12	12-293	12 mA	4.42	7.33	5.19	8.61	33	55	36	60	TTL level tri-state with pull-up
ONUT16	12-295	16 mA	3.54	5.88	4.31	7.16	24	41	27	45	TTL level tri-state with pull-up
ONUC02	12-297	2 mA	30.8	51.1	20.3	33.7	266	442	166	276	CMOS level tri-state with pull-up
ONUC04	12-299	4 mA	16.0	26.6	11.2	18.6	133	220	83	138	CMOS level tri-state with pull-up

Name	Page	Output Drive	Timing Information (CL = 100pF)								Description
			tPLH (ns)		tPHL (ns)		ΔtPLH (ps/pF)		ΔtPHL (ps/pF)		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
ONUC06	12-301	6 mA	10.7	17.8	7.49	12.4	89	147	55	91	CMOS level tri-state with pull-up
ONUC08	12-303	8 mA	8.09	13.4	6.09	10.1	64	107	41	69	CMOS level tri-state with pull-up
ONUC12	12-305	12 mA	5.47	9.08	4.29	7.13	42	69	28	46	CMOS level tri-state with pull-up
ONUC16	12-307	16 mA	4.43	7.36	3.69	6.13	31	52	21	34	CMOS level tri-state with pull-up
BSTTD02	13-1	2 mA	25.2	41.8	28.2	46.9	206	341	216	358	Bidirectional TTL output with pull-down. Output drive is 2 mA with slew-rate
BSTTD04	13-3	4 mA	13.9	23.1	16.4	27.3	103	171			Bidirectional TTL output with pull-down. Output drive is 4 mA with slew-rate
BSTTD06	13-5	6 mA	10.4	17.2	12.7	21.1	68	114	74	123	Bidirectional TTL output with pull-down. Output drive is 6 mA with slew-rate
BSTTD08	13-7	8 mA	8.74	14.5	11.0	18.3	51	85	57	94	Bidirectional TTL output with pull-down. Output drive is 8 mA with slew-rate
BSTTD12	13-9	12 mA	6.49	10.7	8.30	13.7	33	55	40	66	Bidirectional TTL output with pull-down. Output drive is 12 mA with slew-rate
BSTTD16	13-11	16 mA	5.63	9.35	7.17	11.9	25	42	32	53	Bidirectional TTL output with pull-down. Output drive is 16 mA with slew-rate
BSTTN02	13-13	2 mA	25.1	41.7	28.3	47.1	205	341	217	360	Bidirectional TTL output. Output drive is 2 mA with slew-rate
BSTTN04	13-15	4 mA	13.9	23.1	16.5	27.4	103	170	109	180	Bidirectional TTL output. Output drive is 4 mA with slew-rate
BSTTN06	13-17	6 mA	10.3	17.2	12.7	21.1	68	114	74	123	Bidirectional TTL output. Output drive is 6 mA with slew-rate
BSTTN08	13-19	8 mA	8.73	14.4	11.0	18.3	51	85	57	94	Bidirectional TTL output. Output drive is 8 mA with slew-rate
BSTTN12	13-21	12 mA	6.49	10.7	8.31	13.7	33	55	40	66	Bidirectional TTL output. Output drive is 12 mA with slew-rate
BSTTN16	13-23	16 mA	5.63	9.35	7.17	11.9	25	42	32	53	Bidirectional TTL output. Output drive is 16 mA with slew-rate
BSTTU02	13-25	2 mA	25.0	41.5	28.4	47.1	204	339	217	360	Bidirectional TTL output with pull-up. Output drive is 2 mA with slew-rate
BSTTU04	13-27	4 mA	13.9	23.1	16.5	27.4	102	170	109	181	Bidirectional TTL output with pull-up. Output drive is 4 mA with slew-rate
BSTTU06	13-29	6 mA	10.3	17.2	12.7	21.2	68	113	74	123	Bidirectional TTL output with pull-up. Output drive is 6 mA with slew-rate
BSTTU08	13-31	8 mA	8.72	14.4	11.0	18.3	51	85	57	94	Bidirectional TTL output with pull-up. Output drive is 8 mA with slew-rate
BSTTU12	13-33	12 mA	6.49	10.7	8.31	13.7	33	55	40	66	Bidirectional TTL output with pull-up. Output drive is 12 mA with slew-rate
BSTTU16	13-35	16 mA	5.63	9.35	7.17	11.9	25	42	32	53	Bidirectional TTL output with pull-up. Output drive is 16 mA with slew-rate
BSTCD02	13-37	2 mA	32.3	53.6	22.4	37.2	268	445	165	274	Bidirectional CMOS output with pull-down. Output drive is 2 mA with slew-rate
BSTCD04	13-39	4 mA	17.6	29.2	13.6	22.6	133	221	83	138	Bidirectional CMOS output with pull-down. Output drive is 4 mA with slew-rate
BSTCD06	13-41	6 mA	13.0	21.6	10.9	18.1	89	148	56	94	Bidirectional CMOS output with pull-down. Output drive is 6 mA with slew-rate
BSTCD08	13-43	8 mA	10.6	17.7	9.78	16.2	65	107	44	73	Bidirectional CMOS output with pull-down. Output drive is 8 mA with slew-rate
BSTCD12	13-45	12 mA	8.04	13.3	7.41	12.3	42	70	31	52	Bidirectional CMOS output with pull-down. Output drive is 12 mA with slew-rate
BSTCD16	13-47	16 mA	7.10	11.7	6.45	10.7	33	54	26	42	Bidirectional CMOS output with pull-down. Output drive is 16 mA with slew-rate

Name	Page	Output Drive	Timing Information (CL = 100pF)								Description
			tPLH (ns)		tPHL (ns)		ΔtPLH (ps/pF)		ΔtPHL (ps/pF)		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
BSTCN02	13-49	2 mA	32.2	53.4	22.5	37.4	267	444	166	276	Bidirectional CMOS output. Output drive is 2 mA with slew-rate
BSTCN04	13-51	4 mA	17.6	29.2	13.6	22.6	133	221	83	138	Bidirectional CMOS output. Output drive is 4 mA with slew-rate
BSTCN06	13-53	6 mA	13.0	21.6	10.9	18.1	89	148	57	94	Bidirectional CMOS output. Output drive is 6 mA with slew-rate
BSTCN08	13-55	8 mA	10.6	17.6	9.79	16.2	65	107	44	73	Bidirectional CMOS output. Output drive is 8 mA with slew-rate
BSTCN12	13-57	12 mA	8.04	13.3	7.41	12.3	42	70	31	52	Bidirectional CMOS output. Output drive is 12 mA with slew-rate
BSTCN16	13-59	16 mA	7.10	11.7	6.45	10.7	33	54	26	42	Bidirectional CMOS output. Output drive is 16 mA with slew-rate
BSTCU02	13-61	2 mA	32.1	53.3	22.5	37.4	266	442	166	276	Bidirectional CMOS output with pull-up. Output drive is 2 mA with slew-rate
BSTCU04	13-63	4 mA	17.5	29.1	13.6	22.7	133	220	83	138	Bidirectional CMOS output with pull-up. Output drive is 4 mA with slew-rate
BSTCU06	13-65	6 mA	13.0	21.6	10.9	18.2	89	147	57	94	Bidirectional CMOS output with pull-up. Output drive is 6 mA with slew-rate
BSTCU08	13-67	8 mA	10.6	17.6	9.79	16.2	65	107	44	73	Bidirectional CMOS output with pull-up. Output drive is 8 mA with slew-rate
BSTCU12	13-69	12 mA	8.03	13.3	7.41	12.3	42	70	31	52	Bidirectional CMOS output with pull-up. Output drive is 12 mA with slew-rate
BSTCU16	13-71	16 mA	7.09	11.7	6.45	10.7	33	54	26	42	Bidirectional CMOS output with pull-up. Output drive is 16 mA with slew-rate
BSNTU02	13-73	2 mA			27.5	45.7			220	365	N-channel open drain bidirectional TTL output with pull-up. Output drive is 2 mA with slew-rate
BSNTU04	13-74	4 mA			15.4	25.6			110	182	N-channel open drain bidirectional TTL output with pull-up. Output drive is 4 mA with slew-rate
BSNTU06	13-75	6 mA			11.5	19.1			74	122	N-channel open drain bidirectional TTL output with pull-up. Output drive is 6 mA with slew-rate
BSNTU08	13-76	8 mA			9.67	16.0			56	93	N-channel open drain bidirectional TTL output with pull-up. Output drive is 8 mA with slew-rate
BSNTU12	13-77	12 mA			7.63	12.6			40	66	N-channel open drain bidirectional TTL output with pull-up. Output drive is 12 mA with slew-rate
BSNTU16	13-78	16 mA			6.68	11.0			32	53	N-channel open drain bidirectional TTL output with pull-up. Output drive is 16 mA with slew-rate
BSNCU02	13-79	2 mA			21.5	35.7			166	276	N-channel open drain bidirectional CMOS output with pull-up. Output drive is 2 mA with slew-rate
BSNCU04	13-80	4 mA			12.4	20.6			83	138	N-channel open drain bidirectional CMOS output with pull-up. Output drive is 4 mA with slew-rate
BSNCU06	13-81	6 mA			9.49	15.7			56	93	N-channel open drain bidirectional CMOS output with pull-up. Output drive is 6 mA with slew-rate
BSNCU08	13-82	8 mA			8.10	13.4			43	72	N-channel open drain bidirectional CMOS output with pull-up. Output drive is 8 mA with slew-rate
BSNCU12	13-83	12 mA			6.52	10.8			31	51	N-channel open drain bidirectional CMOS output with pull-up. Output drive is 12 mA with slew-rate
BSNCU16	13-84	16 mA			5.78	9.60			25	42	N-channel open drain bidirectional CMOS output with pull-up. Output drive is 16 mA with slew-rate
BSPTD02	13-85	2 mA	24.7	41.0			206	341			P-channel open drain bidirectional TTL output with pull-down. Output drive is 2 mA with slew-rate
BSPTD04	13-86	4 mA	13.4	22.2			103	170			P-channel open drain bidirectional TTL output with pull-down. Output drive is 4 mA with slew-rate

Name	Page	Output Drive	Timing Information (CL = 100pF)								Description
			tPLH (ns)		tPHL (ns)		ΔtPLH (ps/pF)		ΔtPHL (ps/pF)		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
BSPTD06	13-87	6 mA	9.73	16.1			68	114			P-channel open drain bidirectional TTL output with pull-down. Output drive is 6 mA with slew-rate
BSPTD08	13-88	8 mA	7.97	13.2			51	85			P-channel open drain bidirectional TTL output with pull-down. Output drive is 8 mA with slew-rate
BSPTD12	13-89	12 mA	6.09	10.1			33	55			P-channel open drain bidirectional TTL output with pull-down. Output drive is 12 mA with slew-rate
BSPTD16	13-90	16 mA	5.31	8.81			25	42			P-channel open drain bidirectional TTL output with pull-down. Output drive is 16 mA with slew-rate
BSPCD02	13-91	2 mA	31.8	52.7			268	445			P-channel open drain bidirectional CMOS output with pull-down. Output drive is 2 mA with slew-rate
BSPCD04	13-92	4 mA	17.0	28.2			133	221			P-channel open drain bidirectional CMOS output with pull-down. Output drive is 4 mA with slew-rate
BSPCD06	13-93	6 mA	12.3	20.5			89	148			P-channel open drain bidirectional CMOS output with pull-down. Output drive is 6 mA with slew-rate
BSPCD08	13-94	8 mA	9.86	16.3			65	107			P-channel open drain bidirectional CMOS output with pull-down. Output drive is 8 mA with slew-rate
BSPCD12	13-95	12 mA	7.61	12.6							P-channel open drain bidirectional CMOS output with pull-down. Output drive is 12 mA with slew-rate
BSPCD16	13-96	16 mA	6.77	11.2			32	54			P-channel open drain bidirectional CMOS output with pull-down. Output drive is 16 mA with slew-rate
BMTTD12	13-97	12 mA	5.49	9.11	6.99	11.6	33	55	37	62	Bidirectional TTL output with pull-down. Output drive is 12 mA with moderate slew-rate
BMTTD16	13-99	16 mA	4.47	7.43	5.76	9.57	24	41	29	48	Bidirectional TTL output with pull-down. Output drive is 16 mA with moderate slew-rate
BMTTN12	13-101	12 mA	5.49	9.11	6.99	11.6	33	55	38	62	Bidirectional TTL output. Output drive is 12 mA with moderate slew-rate
BMTTN16	13-103	16 mA	4.47	7.43	5.76	9.57	24	41	29	48	Bidirectional TTL output. Output drive is 16 mA with moderate slew-rate
BMTTU12	13-105	12 mA	5.48	9.09	6.99	11.6	33	55	38	62	Bidirectional TTL output with pull-up. Output drive is 12 mA with moderate slew-rate
BMTTU16	13-107	16 mA	4.47	7.43	5.76	9.57	24	41	29	48	Bidirectional TTL output with pull-up. Output drive is 16 mA with moderate slew-rate
BMTCD12	13-109	12 mA	6.75	11.2	6.20	10.3	42	69	29	48	Bidirectional CMOS output with pull-down. Output drive is 12 mA with moderate slew-rate
BMTCD16	13-111	16 mA	5.61	9.32	5.15	8.56	31	52	22	37	Bidirectional CMOS output with pull-down. Output drive is 16 mA with moderate slew-rate
BMTCN12	13-113	12 mA	6.75	11.2	6.20	10.3	42	69	29	48	Bidirectional CMOS output. Output drive is 12 mA with moderate slew-rate
BMTCN16	13-115	16 mA	5.61	9.32	5.15	8.56	31	52	22	37	Bidirectional CMOS output. Output drive is 16 mA with moderate slew-rate
BMTCU12	13-117	12 mA	6.75	11.2	6.20	10.3	42	69	29	48	Bidirectional CMOS output with pull-up. Output drive is 12 mA with moderate slew-rate
BMTCU16	13-119	16 mA	5.61	9.32	5.15	8.56	31	52	23	37	Bidirectional CMOS output with pull-up. Output drive is 16 mA with moderate slew-rate
BMNTU12	13-121	-			6.24	10.3			37	62	PARAMETER
BMNTU16	13-122	-			4.77	7.91			28	47	PARAMETER
BMNCU12	13-123	-			5.20	8.63			28	47	PARAMETER
BMNCU16	13-124	-			3.97	6.60			22	36	PARAMETER
BMPTD12	13-125	12 mA	5.06	8.40			33	55			P-channel open drain bidirectional TTL output with pull-down. Output drive is 12 mA with moderate slew-rate
BMPTD16	13-126	16 mA	3.91	6.48			24	41			P-channel open drain bidirectional TTL output with pull-down. Output drive is 16 mA with moderate slew-rate
BMPCD12	13-127	-	6.31	10.4			42	69			PARAMETER

Name	Page	Output Drive	Timing Information (CL = 100pF)								Description
			tPLH (ns)		tPHL (ns)		ΔtPLH (ps/pF)		ΔtPHL (ps/pF)		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
BMPCD16	13-128	16 mA	4.95	8.22			31	52			P-channel open drain bidirectional CMOS output with pull-down. Output drive is 16 mA with moderate slew-rate
BNTTD02	13-129	2 mA	24.0	39.8	26.0	43.2	206	341	216	358	Bidirectional TTL output with pull-down. Output drive is 2 mA
BNTTD04	13-131	4 mA	12.6	20.9	14.0	23.3	103	170	108	179	Bidirectional TTL output with pull-down. Output drive is 4 mA
BNTTD06	13-133	6 mA	8.42	13.9	9.37	15.5	68	114	73	120	Bidirectional TTL output with pull-down. Output drive is 6 mA
BNTTD08	13-135	8 mA	6.56	10.9	7.45	12.3	51	85	54	90	Bidirectional TTL output with pull-down. Output drive is 8 mA
BNTTD12	13-137	12 mA	4.43	7.35	5.19	8.61	33	55			Bidirectional TTL output with pull-down. Output drive is 12 mA
BNTTD16	13-139	16 mA	3.54	5.88	4.31	7.16	24	41	27	45	Bidirectional TTL output with pull-down. Output drive is 16 mA
BNTTN02	13-141	2 mA	23.9	39.7	26.1	43.4	205	341	217	360	Bidirectional TTL output. Output drive is 2 mA
BNTTN04	13-143	4 mA	12.6	20.9	14.1	23.4	103	170	108	180	Bidirectional TTL output. Output drive is 4 mA
BNTTN06	13-145	6 mA	8.40	13.9	9.38	15.5	68	114	73	121	Bidirectional TTL output. Output drive is 6 mA
BNTTN08	13-147	8 mA	6.55	10.8	7.46	12.3	51	85	54	90	Bidirectional TTL output. Output drive is 8 mA
BNTTN12	13-149	12 mA	4.43	7.35	5.19	8.61	33	55	36	60	Bidirectional TTL output. Output drive is 12 mA
BNTTN16	13-151	16 mA	3.54	5.88	4.31	7.16	24	41	27	45	Bidirectional TTL output. Output drive is 16 mA
BNTTU02	13-153	2 mA	23.8	39.5	26.2	43.5	204	339	217	360	Bidirectional TTL output with pull-up. Output drive is 2 mA
BNTTU04	13-155	4 mA	12.5	20.8	14.1	23.4	102	170	108	180	Bidirectional TTL output with pull-up. Output drive is 4 mA
BNTTU06	13-157	6 mA	8.39	13.9	9.38	15.5	68	113	73	121	Bidirectional TTL output with pull-up. Output drive is 6 mA
BNTTU08	13-159	8 mA	6.55	10.8	7.46	12.3	51	85	54	90	Bidirectional TTL output with pull-up. Output drive is 8 mA
BNTTU12	13-161	12 mA	4.42	7.33	5.19	8.61	33	55	36	60	Bidirectional TTL output with pull-up. Output drive is 12 mA
BNTTU16	13-163	16 mA	3.54	5.88	4.31	7.16	24	41	27	45	Bidirectional TTL output with pull-up. Output drive is 16 mA
BNTCD02	13-165	2 mA	31.0	51.4	20.2	33.6	268	445	165	274	Bidirectional CMOS output with pull-down. Output drive is 2 mA
BNTCD04	13-167	4 mA	16.1	26.7	11.2	18.6	133	221	83	137	Bidirectional CMOS output with pull-down. Output drive is 4 mA
BNTCD06	13-169	6 mA	10.7	17.8	7.47	12.4	89	148	55	91	Bidirectional CMOS output with pull-down. Output drive is 6 mA
BNTCD08	13-171	8 mA	8.11	13.4	6.08	10.1	64	107	41	68	Bidirectional CMOS output with pull-down. Output drive is 8 mA
BNTCD12	13-173	12 mA	5.47	9.08	4.29	7.13	42	69	28	46	Bidirectional CMOS output with pull-down. Output drive is 12 mA
BNTCD16	13-175	16 mA	4.43	7.36	3.69	6.13	31	52	21	34	Bidirectional CMOS output with pull-down. Output drive is 16 mA
BNTCN02	13-177	2 mA	30.9	51.3	20.3	33.7	267	444	166	275	Bidirectional CMOS output. Output drive is 2 mA
BNTCN04	13-179	4 mA	16.0	26.6	11.2	18.6	133	221	83	137	Bidirectional CMOS output. Output drive is 4 mA
BNTCN06	13-181	6 mA	10.7	17.8	7.48	12.4	89	147	55	91	Bidirectional CMOS output. Output drive is 6 mA
BNTCN08	13-183	8 mA	8.09	13.4	6.08	10.1	64	107	41	69	Bidirectional CMOS output. Output drive is 8 mA
BNTCN12	13-185	12 mA	5.47	9.08	4.29	7.13	42	69	28	46	Bidirectional CMOS output. Output drive is 12 mA
BNTCN16	13-187	16 mA	4.43	7.35	3.69	6.13	31	52	21	34	Bidirectional CMOS output. Output drive is 16 mA
BNTCU02	13-189	2 mA	30.8	51.1	20.3	33.7	266	442	166	276	Bidirectional CMOS output with pull-up. Output drive is 2 mA
BNTCU04	13-191	4 mA	16.0	26.6	11.2	18.6	133	220	83	138	Bidirectional CMOS output with pull-up. Output drive is 4 mA
BNTCU06	13-193	6 mA	10.7	17.8	7.49	12.4	89	147	55	91	Bidirectional CMOS output with pull-up. Output drive is 6 mA

Name	Page	Output Drive	Timing Information (CL = 100pF)								Description
			tPLH (ns)		tPHL (ns)		ΔtPLH (ps/pF)		ΔtPHL (ps/pF)		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
BNTCU08	13-195	8 mA	8.09	13.4	6.09	10.1	64	107	41	69	Bidirectional CMOS output with pull-up. Output drive is 8 mA
BNTCU12	13-197	12 mA	5.47	9.08	4.29	7.13	42	69	28	46	Bidirectional CMOS output with pull-up. Output drive is 12 mA
BNTCU16	13-199	16 mA	4.43	7.36	3.69	6.13	31	52	21	34	Bidirectional CMOS output with pull-up. Output drive is 16 mA
BNNTU02	13-201	2 mA			25.4	42.2					N-channel open drain bidirectional TTL output with pull-up. Output drive is 2 mA
BNNTU04	13-202	4 mA			12.8	21.2			110	182	N-channel open drain bidirectional TTL output with pull-up. Output drive is 4 mA
BNNTU06	13-203	6 mA			8.70	14.4			73	121	N-channel open drain bidirectional TTL output with pull-up. Output drive is 6 mA
BNNTU08	13-204	8 mA			6.61	10.9					N-channel open drain bidirectional TTL output with pull-up. Output drive is 8 mA
BNNTU12	13-205	12 mA			4.55	7.55			36	60	N-channel open drain bidirectional TTL output with pull-up. Output drive is 12 mA
BNNTU16	13-206	16 mA			3.57	5.93			27	45	N-channel open drain bidirectional TTL output with pull-up. Output drive is 16 mA
BNNCU02	13-207	2 mA			19.4	32.3			166	276	N-channel open drain bidirectional CMOS output with pull-up. Output drive is 2 mA
BNNCU04	13-208	4 mA			9.81	16.2			83	138	N-channel open drain bidirectional CMOS output with pull-up. Output drive is 4 mA
BNNCU06	13-209	6 mA			6.71	11.1			55	91	N-channel open drain bidirectional CMOS output with pull-up. Output drive is 6 mA
BNNCU08	13-210	8 mA			5.12	8.51			41	69	N-channel open drain bidirectional CMOS output with pull-up. Output drive is 8 mA
BNNCU12	13-211	12 mA			3.56	5.91			27	46	N-channel open drain bidirectional CMOS output with pull-up. Output drive is 12 mA
BNNCU16	13-212	16 mA			2.83	4.69			21	34	N-channel open drain bidirectional CMOS output with pull-up. Output drive is 16 mA
BNPTD02	13-213	2 mA	23.5	39.0			206	341			P-channel open drain bidirectional TTL output with pull-down. Output drive is 2 mA
BNPTD04	13-214	4 mA	11.8	19.6			103	170			P-channel open drain bidirectional TTL output with pull-down. Output drive is 4 mA
BNPTD06	13-215	6 mA	8.01	13.2			68	114			P-channel open drain bidirectional TTL output with pull-down. Output drive is 6 mA
BNPTD08	13-216	8 mA	6.07	10.0			51	85			P-channel open drain bidirectional TTL output with pull-down. Output drive is 8 mA
BNPTD12	13-217	12 mA	4.02	6.68			33	55			P-channel open drain bidirectional TTL output with pull-down. Output drive is 12 mA
BNPTD16	13-218	16 mA	3.08	5.11			24	41			P-channel open drain bidirectional TTL output with pull-down. Output drive is 16 mA
BNPCD02	13-219	2 mA	30.4	50.5			268	445			P-channel open drain bidirectional CMOS output with pull-down. Output drive is 2 mA
BNPCD04	13-220	4 mA	15.2	25.3			133	221			P-channel open drain bidirectional CMOS output with pull-down. Output drive is 4 mA
BNPCD06	13-221	6 mA	10.3	17.1			89	148			P-channel open drain bidirectional CMOS output with pull-down. Output drive is 6 mA
BNPCD08	13-222	8 mA	7.56	12.5			64	107			P-channel open drain bidirectional CMOS output with pull-down. Output drive is 8 mA
BNPCD12	13-223	12 mA	5.01	8.32			42	69			P-channel open drain bidirectional CMOS output with pull-down. Output drive is 12 mA

Name	Page	Output Drive	Timing Information (CL = 100pF)								Description
			tPLH (ns)		tPHL (ns)		Δ tPLH (ps/pF)		Δ tPHL (ps/pF)		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
BNPCD16	13-224	16 mA	3.89	6.46			31	52			P-channel open drain bidirectional CMOS output with pull-down. Output drive is 16 mA



QYH500

Library

Data

Sheet

— Military

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Library Summary

Name	Page	Drive	Cells	Timing Information								Description
				tPLH (ns)		tPHL (ns)		ΔtPLH (ns/pF)		ΔtPHL (ns/pF)		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
AD2001	5-1	1	2	0.53	1.09	0.55	1.13	0.74	1.52	0.57	1.17	Z = A1*A2
AD2101	5-2	1	2	0.37	0.76	0.46	0.95	1.44	2.97	0.54	1.11	Z = A1*NOT BN
AD2002	5-3	2	2	0.61	1.26	0.62	1.28	0.38	0.78	0.32	0.66	Z = A1*A2
AD3001	5-4	1	2	0.78	1.61	0.67	1.38	0.75	1.54	0.58	1.19	Z = A1*A2*A3
AD3002	5-5	2	3	0.90	1.85	0.75	1.54	0.41	0.84	0.33	0.68	Z = A1*A2*A3
AD4001	5-6	1	3	1.12	2.31	0.79	1.63	0.78	1.61	0.60	1.24	Z = A1*A2*A3*A4
AD4002	5-7	2	3	1.24	2.55	0.83	1.71	0.43	0.89	0.35	0.72	Z = A1*A2*A3*A4
AD5001	5-8	1	3	1.53	3.15	0.89	1.83	0.81	1.67	0.62	1.28	Z = A1*A2*A3*A4*A5
AD6001	5-9	1	4	0.96	1.98	0.75	1.54	1.44	2.97	0.58	1.19	Z = A1*A2*A3*A4*A5*A6
AD7001	5-10	1	5	1.26	2.60	0.85	1.75	1.43	2.95	0.60	1.24	Z = A1*A2*A3*A4*A5*A6*A7
AD8001	5-11	1	5	1.26	2.60	0.84	1.73	1.43	2.95	0.60	1.24	Z = A1*A2*A3*A4*A5*A6*A7*A8
EN2001	5-12	1	3	0.66	1.36	0.83	1.71	0.74	1.52	0.63	1.30	Z = NOT(A1∞A2)
EN2002	5-13	2	4	0.66	1.36	1.06	2.18	0.38	0.78	0.40	0.82	Z = NOT(A1∞A2)
EN3001	5-14	1	6	1.65	3.40	2.13	4.39	0.74	1.52	0.64	1.32	Z = NOT(A1∞A2∞A3)
EX2001	5-15	1	3	0.88	1.81	1.07	2.20	0.75	1.54	0.57	1.17	Z = A1∞A2
EX2002	5-16	2	4	0.94	1.94	1.12	2.31	0.40	0.82	0.33	0.68	Z = A1∞A2
EX3001	5-17	1	6	2.01	4.14	2.08	4.28	0.75	1.54	0.57	1.17	Z = A1∞A2∞A3
IT1001	5-18	1	4	0.72	1.48	0.76	1.57	0.75	1.54	0.62	1.28	Inverting 3-state buffer the enable input is active low
IT1002	5-19	2	5	0.81	1.67	0.82	1.69	0.40	0.82	0.40	0.82	Inverting 3-state buffer the enable input is active low
IT1004	5-20	4	7	0.89	1.83	1.00	2.06	0.26	0.54	0.30	0.62	Inverting 3-state buffer the enable input is active low
IT1101	5-21	1	4	0.53	1.09	1.00	2.06	0.75	1.54	0.61	1.26	Inverting 3-state buffer the enable input is active high
IT1102	5-22	2	5	0.58	1.19	1.07	2.20	0.40	0.82	0.40	0.82	Inverting 3-state buffer the enable input is active high
IT1104	5-23	4	7	0.66	1.36	1.24	2.55	0.26	0.54	0.30	0.62	Inverting 3-state buffer the enable input is active high
IV1001	5-24	1	1	0.13	0.27	0.22	0.45	0.74	1.52	0.54	1.11	Z = NOT A
IV1002	5-25	2	1	0.15	0.31	0.22	0.45	0.36	0.74	0.27	0.56	Z = NOT A
IV1003	5-26	3	2	0.15	0.31	0.20	0.41	0.24	0.49	0.19	0.39	Z = NOT A
IV1004	5-27	4	2	0.15	0.31	0.19	0.39	0.18	0.37	0.15	0.31	Z = NOT A
IV1005	5-28	5	3	0.15	0.31	0.18	0.37	0.14	0.29	0.13	0.27	Z = NOT A
IV1006	5-29	6	3	0.13	0.27	0.18	0.37	0.12	0.25	0.11	0.23	Z = NOT A
IV1007	5-30	7	4	0.13	0.27	0.16	0.33	0.10	0.21	0.10	0.21	Z = NOT A
IV1008	5-31	8	4	0.13	0.27	0.22	0.45	0.09	0.19	0.07	0.14	Z = NOT A
IV1010	5-32	10	5	0.13	0.27	0.20	0.41	0.07	0.14	0.05	0.10	Z = NOT A
IV1020	5-33	20	10	0.13	0.27	0.18	0.37	0.03	0.06	0.03	0.06	Z = NOT A
IV1030	5-34	30	15	0.13	0.27	0.19	0.39	0.02	0.04	0.02	0.04	Z = NOT A
ND2001	5-35	1	1	0.23	0.47	0.28	0.58	0.75	1.54	0.92	1.90	Z = NOT(A1*A2)
ND2101	5-36	1	2	0.37	0.76	0.36	0.74	0.76	1.57	0.97	2.00	Z = NOT(A1*NOT BN)
ND2002	5-37	2	2	0.23	0.47	0.28	0.58	0.37	0.76	0.46	0.95	Z = NOT(A1*A2)
ND3001	5-38	1	2	0.32	0.66	0.45	0.93	0.75	1.54	1.30	2.68	Z = NOT(A1*A2*A3)
ND3002	5-39	2	3	0.32	0.66	0.45	0.93	0.38	0.78	0.65	1.34	Z = NOT(A1*A2*A3)
ND3101	5-40	1	2	0.40	0.82	0.45	0.93	0.76	1.57	1.31	2.70	Z = NOT(A1*A2*NOT BN)
ND4001	5-41	1	2	0.40	0.82	0.72	1.48	0.77	1.59	1.69	3.48	Z = NOT(A1*A2*A3*A4)
ND4002	5-42	2	4	0.37	0.76	0.70	1.44	0.40	0.82	0.84	1.73	Z = NOT(A1*A2*A3*A4)
ND5001	5-43	1	3	0.43	0.89	1.02	2.10	0.80	1.65	2.07	4.26	Z = NOT(A1*A2*A3*A4*A5)
ND5002	5-44	2	5	0.42	0.87	1.02	2.10	0.41	0.84	1.05	2.16	Z = NOT(A1*A2*A3*A4*A5)

Name	Page	Drive	Cells	Timing Information								Description
				tPLH (ns)		tPHL (ns)		ΔtPLH (ns/pF)		ΔtPHL (ns/pF)		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
ND6001	5-45	1	5	0.85	1.75	1.37	2.82	0.75	1.54	0.59	1.22	Z = NOT(A1*A2*A3*A4*A5*A6)
ND6002	5-46	2	5	0.96	1.98	1.52	3.13	0.37	0.76	0.36	0.74	Z = NOT(A1*A2*A3*A4*A5*A6)
ND7001	5-47	1	5	0.97	2.00	1.67	3.44	0.74	1.52	0.60	1.24	Z = NOT(A1*A2*A3*A4*A5*A6*A7)
ND7002	5-48	2	6	1.05	2.16	1.80	3.71	0.37	0.76	0.36	0.74	Z = NOT(A1*A2*A3*A4*A5*A6*A7)
ND8001	5-49	1	6	0.97	2.00	1.67	3.44	0.74	1.52	0.60	1.24	Z = NOT(A1*A2*A3*A4*A5*A6*A7*A8)
ND8002	5-50	2	6	1.06	2.18	1.83	3.77	0.37	0.76	0.36	0.74	Z = NOT(A1*A2*A3*A4*A5*A6*A7*A8)
NR2001	5-51	1	1	0.34	0.70	0.28	0.58	1.43	2.95	0.55	1.13	Z = NOT(A1+A2)
NR2101	5-52	1	2	0.37	0.76	0.46	0.95	1.44	2.97	0.54	1.11	Z = NOT(A1+NOT BN)
NR2002	5-53	2	2	0.34	0.70	0.26	0.54	0.72	1.48	0.28	0.58	Z = NOT(A1+A2)
NR3001	5-54	1	2	0.67	1.38	0.31	0.64	2.14	4.41	0.57	1.17	Z = NOT(A1+A2+A3)
NR3002	5-55	2	3	0.65	1.34	0.29	0.60	1.07	2.20	0.29	0.60	Z = NOT(A1+A2+A3)
NR3101	5-56	1	2	0.46	0.95	0.46	0.95	2.15	4.43	0.54	1.11	Z = NOT(A1+A2+NOT BN)
NR4001	5-57	1	2	1.18	2.43	0.32	0.66	2.83	5.83	0.58	1.19	Z = NOT(A1+A2+A3+A4)
NR4002	5-58	2	4	1.16	2.39	0.31	0.64	1.42	2.93	0.30	0.62	Z = NOT(A1+A2+A3+A4)
NR5001	5-59	1	3	1.77	3.65	0.34	0.70	3.54	7.29	0.59	1.22	Z = NOT(A1+A2+A3+A4+A5)
NR5002	5-60	2	5	1.73	3.56	0.32	0.66	1.77	3.65	0.30	0.62	Z = NOT(A1+A2+A3+A4+A5)
NR6001	5-61	1	5	1.53	3.15	0.89	1.83	0.75	1.54	0.57	1.17	Z = NOT(A1+A2+A3+A4+A5+A6)
NR6002	5-62	2	5	1.65	3.40	0.97	2.00	0.38	0.78	0.31	0.64	Z = NOT(A1+A2+A3+A4+A5+A6)
NR7001	5-63	1	5	2.20	4.53	0.94	1.94	0.75	1.54	0.57	1.17	Z = NOT(A1+A2+A3+A4+A5+A6+A7)
NR7002	5-64	2	6	2.33	4.80	1.01	2.08	0.40	0.82	0.31	0.64	Z = NOT(A1+A2+A3+A4+A5+A6+A7)
NR8001	5-65	1	6	2.18	4.49	0.93	1.92	0.75	1.54	0.57	1.17	Z = NOT(A1+A2+A3+A4+A5+A6+A7+A8)
NR8002	5-66	2	6	2.31	4.76	1.01	2.08	0.40	0.82	0.31	0.64	Z = NOT(A1+A2+A3+A4+A5+A6+A7+A8)
NT1001	5-67	1	4	0.70	1.44	0.75	1.54	0.75	1.54	0.62	1.28	3-state buffer the enable input is active low
NT1002	5-68	2	5	0.81	1.67	0.81	1.67	0.40	0.82	0.40	0.82	3-state buffer the enable input is active low
NT1004	5-69	4	7	0.89	1.83	0.99	2.04	0.26	0.54	0.30	0.62	3-state buffer the enable input is active low
NT1101	5-70	1	4	0.52	1.07	0.99	2.04	0.75	1.54	0.61	1.26	3-state buffer the enable input is active high
NT1102	5-71	2	5	0.58	1.19	1.07	2.20	0.40	0.82	0.40	0.82	3-state buffer the enable input is active high
NT1104	5-72	4	7	0.66	1.36	1.25	2.58	0.26	0.54	0.29	0.60	3-state buffer the enable input is active high
NV1001	5-73	1	1	0.35	0.72	0.39	0.80	0.74	1.52	0.55	1.13	Z = A
NV1002	5-74	2	2	0.41	0.84	0.47	0.97	0.37	0.76	0.30	0.62	Z = A
NV1003	5-75	3	2	0.47	0.97	0.58	1.19	0.25	0.52	0.22	0.45	Z = A
NV1004	5-76	4	3	0.41	0.84	0.46	0.95	0.19	0.39	0.16	0.33	Z = A
NV1005	5-77	5	4	0.43	0.89	0.48	0.99	0.15	0.31	0.14	0.29	Z = A
NV1006	5-78	6	4	0.46	0.95	0.54	1.11	0.13	0.27	0.13	0.27	Z = A
NV1007	5-79	7	5	0.42	0.87	0.46	0.95	0.11	0.23	0.10	0.21	Z = A
NV1008	5-80	8	6	0.41	0.84	0.47	0.97	0.09	0.19	0.07	0.14	Z = A
NV1010	5-81	10	7	0.43	0.89	0.53	1.09	0.07	0.14	0.06	0.12	Z = A
NV1020	5-82	20	13	0.48	0.99	0.58	1.19	0.04	0.08	0.03	0.06	Z = A
NV1030	5-83	30	19	0.53	1.09	0.61	1.26	0.02	0.04	0.02	0.04	Z = A
OR2001	5-84	1	2	0.43	0.89	0.78	1.61	0.75	1.54	0.60	1.24	Z = A1+A2
OR2101	5-85	1	2	0.37	0.76	0.36	0.74	0.76	1.57	0.97	2.00	Z = A1+NOT BN
OR2002	5-86	2	2	0.52	1.07	0.90	1.85	0.37	0.76	0.36	0.74	Z = A1+A2
OR3001	5-87	1	2	0.47	0.97	1.29	2.66	0.75	1.54	0.67	1.38	Z = A1+A2+A3
OR3002	5-88	2	3	0.54	1.11	1.43	2.95	0.38	0.78	0.42	0.87	Z = A1+A2+A3
OR4001	5-89	1	3	0.53	1.09	1.94	4.00	0.76	1.57	0.76	1.57	Z = A1+A2+A3+A4
OR4002	5-90	2	3	0.58	1.19	2.14	4.41	0.40	0.82	0.49	1.01	Z = A1+A2+A3+A4
OR5001	5-91	1	3	0.54	1.11	2.65	5.46	0.77	1.59	0.85	1.75	Z = A1+A2+A3+A4+A5
OR6001	5-92	1	4	0.59	1.22	1.33	2.74	0.75	1.54	0.95	1.96	Z = A1+A2+A3+A4+A5+A6
OR7001	5-93	1	5	0.61	1.26	1.98	4.08	0.76	1.57	0.98	2.02	Z = A1+A2+A3+A4+A5+A6+A7

Name	Page	Drive	Cells	Timing Information								Description
				tPLH (ns)		tPHL (ns)		ΔtPLH (ns/pF)		ΔtPHL (ns/pF)		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
OR8001	5-94	1	5	0.61	1.26	1.98	4.08	0.76	1.57	0.98	2.02	Z = A1+A2+A3+A4+A5+A6+A7+A8
AN3121	6-1	1	2	0.48	0.99	0.34	0.70	1.45	2.99	0.57	1.17	Z = NOT(A1*A2+B1)
AN4121	6-2	1	2	0.72	1.48	0.37	0.76	1.49	3.07	0.57	1.17	Z = NOT(A1*A2*A3+B1)
AN4131	6-3	1	2	1.02	2.10	0.36	0.74	2.07	4.26	0.58	1.19	Z = NOT(A1*A2+B1+B2)
AN4221	6-4	1	2	0.52	1.07	0.48	0.99	1.08	2.22	0.93	1.92	Z = NOT(A1*A2+B1*B2)
AN5121	6-5	1	3	0.90	1.85	0.39	0.80	1.51	3.11	0.60	1.24	Z = NOT(A1*A2*A3*A4+B1)
AN5231	6-6	1	3	0.93	1.92	0.37	0.76	1.79	3.69	0.60	1.24	Z = NOT(A1*A2+B1*B2+C1)
AN6221	6-7	1	3	0.43	0.89	0.52	1.07	0.97	2.00	1.30	2.68	Z = NOT(A1*A2*A3+B1*B2*B3)
AN6331	6-8	1	3	0.43	0.89	0.35	0.72	1.41	2.90	0.92	1.90	Z = NOT(A1*A2+B1*B2+C1*D2)
AN8221	6-9	1	4	0.53	1.09	0.77	1.59	0.93	1.92	1.69	3.48	Z = NOT(A1*A2*A3*A4+B1*B2*B3*B4)
AN8441	6-10	1	4	0.53	1.09	0.39	0.80	1.76	3.63	0.92	1.90	Z = NOT(A1*A2+B1*B2+C1*C2+D1*D2)
AO3121	6-11	1	2	0.54	1.11	0.96	1.98	0.75	1.54	0.75	1.54	Z = A1*A2+B1
AO4122	6-12	2	3	0.67	1.38	1.44	2.97	0.40	0.82	0.42	0.87	Z = A1*A2*A3+B1
AO4132	6-13	2	3	0.65	1.34	1.70	3.50	0.38	0.78	0.80	1.65	Z = A1*A2+B1+B2
AO4222	6-14	2	3	0.65	1.34	0.85	1.75	0.40	0.82	0.36	0.74	Z = A1*A2+B1*B2
AO5121	6-15	1	3	0.67	1.38	1.60	3.30	0.77	1.59	0.73	1.50	Z = A1*A2*A3*A4+B1
AO5231	6-16	1	3	0.60	1.24	1.54	3.17	0.76	1.57	0.74	1.52	Z = A1*A2+B1*B2+C1
AO6222	6-17	2	4	0.96	1.98	0.96	1.98	0.41	0.84	0.37	0.76	Z = A1*A2*A3+B1*B2*B3
AO6332	6-18	2	4	0.70	1.44	1.12	2.31	0.40	0.82	0.41	0.84	Z = A1*A2+B1*B2+C1*C2
AO8222	6-19	2	5	1.32	2.72	1.03	2.12	0.43	0.89	0.38	0.78	Z = A1*A2*A3*A4+B1*B2*B3*B4
AO8442	6-20	2	5	0.72	1.48	1.26	2.60	0.40	0.82	0.46	0.95	Z = A1*A2+B1*B2+C1*C2+D1*D2
CX0011	6-21	1	3	0.67	1.38	0.66	1.36	0.77	1.59	0.99	2.04	Z = NOT((A1+A2)*NOT(B1*B2))
CX0021	6-22	1	3	0.78	1.61	0.93	1.92	1.49	3.07	0.64	1.32	Z = NOT(A1*A2+NOT(B1+B2))
CX0031	6-23	1	3	1.06	2.18	0.59	1.22	1.78	3.67	0.93	1.92	Minority voter Z = NOT((A*B)+(B*C)+(A*C))
CX0042	6-24	2	4	1.02	2.10	1.77	3.65	0.38	0.78	0.50	1.03	Majority voter Z = (A*B)+(B*C)+(A*C)
OA3121	6-25	1	2	0.62	1.28	0.62	1.28	0.74	1.52	0.74	1.52	Z = (A1+A2)*B1
OA4122	6-26	2	3	0.81	1.67	0.83	1.71	0.41	0.84	0.37	0.76	Z = (A1+A2+A3)*B1
OA4132	6-27	2	3	1.03	2.12	0.84	1.73	0.40	0.82	0.38	0.78	Z = (A1+A2)*B1*B2
OA4222	6-28	2	3	0.64	1.32	0.99	2.04	0.38	0.78	0.37	0.76	Z = (A1+A2)*(B1+B2)
OA5121	6-29	1	3	0.85	1.75	0.84	1.73	0.76	1.57	0.72	1.48	Z = (A1+A2+A3+A4)*B1
OA5231	6-30	1	3	0.84	1.73	0.96	1.98	0.78	1.61	0.62	1.28	Z = ((A1+A2)*(B1+B2))*C1
OA6222	6-31	2	4	0.65	1.34	1.60	3.30	0.40	0.82	0.44	0.91	Z = (A1+A2+A3)*(B1+B2+B3)
OA6332	6-32	2	4	0.77	1.59	1.05	2.16	0.40	0.82	0.38	0.78	Z = (A1+A2)*(B1+B2)*(C1+C2)
OA8222	6-33	2	5	0.66	1.36	2.31	4.76	0.40	0.82	0.52	1.07	Z = (A1+A2+A3+A4)*(B1+B2+B3+B4)
OA8442	6-34	2	5	0.89	1.83	1.09	2.25	0.42	0.87	0.40	0.82	Z = (A1+A2)*(B1+B2)*(C1+C2)*(D1+D2)
ON3121	6-35	1	2	0.31	0.64	0.32	0.66	0.76	1.57	0.97	2.00	Z = NOT((A1+A2)*B1)
ON4121	6-36	1	2	0.36	0.74	0.42	0.87	0.77	1.59	0.98	2.02	Z = NOT((A1+A2+A3)*B1)
ON4131	6-37	1	2	0.39	0.80	0.55	1.13	0.77	1.59	1.34	2.76	Z = NOT((A1+A2)*B1*B2)
ON4221	6-38	1	2	0.40	0.82	0.35	0.72	1.44	2.97	0.72	1.48	Z = NOT((A1+A2)*(B1+B2))
ON5121	6-39	1	3	0.42	0.87	0.48	0.99	0.78	1.61	1.01	2.08	Z = NOT((A1+A2+A3+A4)*B1)
ON5231	6-40	1	3	0.45	0.93	0.52	1.07	0.79	1.63	1.13	2.33	Z = NOT((A1+A2)*(B1+B2)*C1)
ON6221	6-41	1	3	0.78	1.61	0.37	0.76	2.14	4.41	0.68	1.40	Z = NOT((A1+A2+A3)*(B1+B2+B3))
ON6331	6-42	1	3	0.45	0.93	0.41	0.84	1.44	2.97	0.91	1.87	Z = NOT((A1+A2)*(B1+B2)*(C1+C2))
ON8221	6-43	1	4	1.35	2.78	0.39	0.80	2.83	5.83	0.67	1.38	Z = NOT((A1+A2+A3+A4)*(B1+B2+B3+B4))
ON8441	6-44	1	4	0.48	0.99	0.47	0.97	1.44	2.97	1.09	2.25	Z = NOT((A1+A2)*(B1+B2)*(C1+C2)*(D1+D2))
DFNB1	7-1	1	9	1.70	3.50	1.65	3.40	0.75	1.54	0.55	1.13	D Flip-Flop - Negative edge triggered with preset and clear
DFNB2	7-3	2	10	1.86	3.83	1.80	3.71	0.37	0.76	0.31	0.64	D Flip-Flop - Negative edge triggered with preset and clear
DFNC1	7-5	1	8	1.62	3.34	1.56	3.21	0.74	1.52	0.58	1.19	D Flip-Flop - Negative edge triggered with clear only
DFNC2	7-7	2	9	1.72	3.54	1.73	3.56	0.41	0.84	0.32	0.66	D Flip-Flop - Negative edge triggered with clear only

Name	Page	Drive	Cells	Timing Information								Description
				tPLH (ns)		tPHL (ns)		ΔtPLH (ns/pF)		ΔtPHL (ns/pF)		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
DFNN1	7-9	1	7	1.42	2.93	1.37	2.82	0.75	1.54	0.57	1.17	D Flip-Flop - Negative edge triggered
DFNN2	7-10	2	8	1.62	3.34	1.54	3.17	0.34	0.70	0.32	0.66	D Flip-Flop - Negative edge triggered
DFNP1	7-11	1	8	1.27	2.62	1.37	2.82	0.75	1.54	0.57	1.17	D Flip-Flop - Negative edge triggered with preset only
DFNP2	7-13	2	9	1.33	2.74	1.46	3.01	0.40	0.82	0.30	0.62	D Flip-Flop - Negative edge triggered with preset only
DFPB1	7-15	1	9	1.62	3.34	1.70	3.50	0.74	1.52	0.55	1.13	D Flip-Flop - Positive edge triggered with preset and clear
DFPB2	7-17	2	10	1.84	3.79	1.95	4.02	0.38	0.78	0.28	0.58	D Flip-Flop - Positive edge triggered with preset and clear
DFPC1	7-19	1	8	1.56	3.21	1.70	3.50	0.74	1.52	0.57	1.17	D Flip-Flop - Positive edge triggered with clear only
DFPC2	7-21	2	9	1.74	3.58	1.83	3.77	0.38	0.78	0.31	0.64	D Flip-Flop - Positive edge triggered with clear only
DFPN1	7-23	1	7	1.36	2.80	1.46	3.01	0.75	1.54	0.57	1.17	D Flip-Flop - Positive edge triggered
DFPN2	7-24	2	8	1.59	3.28	1.64	3.38	0.37	0.76	0.31	0.64	D Flip-Flop - Positive edge triggered
DFPP1	7-25	1	8	1.21	2.49	1.52	3.13	0.75	1.54	0.57	1.17	D Flip-Flop - Positive edge triggered with preset only
DFPP2	7-27	2	9	1.26	2.60	1.61	3.32	0.40	0.82	0.29	0.60	D Flip-Flop - Positive edge triggered with preset only
JKNB1	7-29	1	11	1.42	2.93	1.42	2.93	0.82	1.69	0.72	1.48	JK Flip-Flop - Negative edge triggered with preset and clear
JKNB2	7-31	2	12	1.49	3.07	1.46	3.01	0.45	0.93	0.38	0.78	JK Flip-Flop - Negative edge triggered with preset and clear
JKNC1	7-33	1	10	1.38	2.84	1.36	2.80	0.82	1.69	0.76	1.57	JK Flip-Flop - Negative edge triggered with clear only
JKNC2	7-35	2	11	1.46	3.01	1.38	2.84	0.45	0.93	0.44	0.91	JK Flip-Flop - Negative edge triggered with clear only
JKNN1	7-37	1	9	1.07	2.20	1.17	2.41	0.75	1.54	0.67	1.38	JK Flip-Flop - Negative edge triggered
JKNN2	7-38	2	10	1.13	2.33	1.14	2.35	0.40	0.82	0.43	0.89	JK Flip-Flop - Negative edge triggered
JKNP1	7-39	1	10	1.19	2.45	1.36	2.80	0.77	1.59	0.74	1.52	JK Flip-Flop - Negative edge triggered with preset only
JKNP2	7-41	2	11	1.26	2.60	1.33	2.74	0.42	0.87	0.47	0.97	JK Flip-Flop - Negative edge triggered with preset only
JKPB1	7-43	1	11	1.47	3.03	1.36	2.80	0.83	1.71	0.74	1.52	JK Flip-Flop - Positive edge triggered with preset and clear
JKPB2	7-45	2	12	1.53	3.15	1.32	2.72	0.46	0.95	0.49	1.01	JK Flip-Flop - Positive edge triggered with preset and clear
JKPC1	7-47	1	10	1.42	2.93	1.30	2.68	0.84	1.73	0.76	1.57	JK Flip-Flop - Positive edge triggered with clear only
JKPC2	7-49	2	11	1.46	3.01	1.30	2.68	0.48	0.99	0.46	0.95	JK Flip-Flop - Positive edge triggered with clear only
JKPN1	7-51	1	9	1.07	2.20	1.19	2.45	0.76	1.57	0.67	1.38	JK Flip-Flop - Positive edge triggered
JKPN2	7-52	2	10	1.17	2.41	1.24	2.55	0.40	0.82	0.37	0.76	JK Flip-Flop - Positive edge triggered
JKPP1	7-53	1	10	1.25	2.58	1.33	2.74	0.78	1.61	0.74	1.52	JK Flip-Flop - Positive edge triggered with preset only
JKPP2	7-55	2	11	1.32	2.72	1.33	2.74	0.41	0.84	0.47	0.97	JK Flip-Flop - Positive edge triggered with preset only
SCNB1	7-57	1	11	1.61	3.32	1.74	3.58	0.74	1.52	0.57	1.17	Scan Flip-Flop - Negative edge triggered with preset and clear
SCNC1	7-59	1	10	1.73	3.56	1.47	3.03	0.74	1.52	0.59	1.22	Scan Flip-Flop - Negative edge triggered with clear only
SCNN1	7-61	1	9	1.36	2.80	1.46	3.01	0.74	1.52	0.57	1.17	Scan Flip-Flop - Negative edge triggered
SCNP1	7-62	1	10	1.37	2.82	1.53	3.15	0.74	1.52	0.57	1.17	Scan Flip-Flop - Negative edge triggered with preset only
SCPB1	7-64	1	11	1.56	3.21	1.84	3.79	0.75	1.54	0.59	1.22	Scan Flip-Flop - Positive edge triggered with preset and clear
SCPC1	7-66	1	10	1.60	3.30	1.73	3.56	0.75	1.54	0.58	1.19	Scan Flip-Flop - Positive edge triggered with clear only
SCPN1	7-68	1	9	1.30	2.68	1.49	3.07	0.74	1.52	0.59	1.22	Scan Flip-Flop - Positive edge triggered
SCPP1	7-69	1	10	1.35	2.78	1.62	3.34	0.73	1.50	0.59	1.22	Scan Flip-Flop - Positive edge triggered with preset only
TFPB1	7-71	1	9	1.82	3.75	1.85	3.81	0.74	1.52	0.60	1.24	T Flip-Flop - Positive edge triggered with preset and clear
TFPB2	7-73	2	10	2.02	4.16	2.04	4.20	0.41	0.84	0.34	0.70	T Flip-Flop - Positive edge triggered with preset and clear
TFPC1	7-75	1	8	1.73	3.56	1.82	3.75	0.81	1.67	0.60	1.24	T Flip-Flop - Positive edge triggered with clear only
TFPC2	7-77	2	9	1.83	3.77	1.94	4.00	0.41	0.84	0.38	0.78	T Flip-Flop - Positive edge triggered with clear only
TFPP1	7-79	1	8	1.33	2.74	1.67	3.44	0.75	1.54	0.60	1.24	T Flip-Flop - Positive edge triggered with preset only
TFPP2	7-81	2	9	1.38	2.84	1.66	3.42	0.38	0.78	0.37	0.76	T Flip-Flop - Positive edge triggered with preset only
LANB1	8-1	1	6	0.77	1.59	0.62	1.28	0.77	1.59	0.58	1.19	Latch - Negative gate with preset and clear
LANB2	8-3	2	7	1.02	2.10	0.75	1.54	0.33	0.68	0.30	0.62	Latch - Negative gate with preset and clear
LANC1	8-5	1	5	0.76	1.57	0.61	1.26	0.77	1.59	0.58	1.19	Latch - Negative gate with clear only
LANC2	8-7	2	6	0.96	1.98	0.67	1.38	0.35	0.72	0.32	0.66	Latch - Negative gate with clear only
LANN1	8-9	1	4	1.06	2.18	1.16	2.39	0.73	1.50	0.55	1.13	Latch - Negative gate
LANN2	8-11	2	5	1.27	2.62	1.29	2.66	0.38	0.78	0.32	0.66	Latch - Negative gate
LANP1	8-13	1	5	0.56	1.15	0.53	1.09	0.81	1.67	0.61	1.26	Latch - Negative gate with preset only

Name	Page	Drive	Cells	Timing Information								Description
				tPLH (ns)		tPHL (ns)		ΔtPLH (ns/pF)		ΔtPHL (ns/pF)		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
LANP2	8-15	2	6	0.78	1.61	0.60	1.24	0.41	0.84	0.34	0.70	Latch - Negative gate with preset only
LAPB1	8-17	1	6	0.83	1.71	0.72	1.48	0.74	1.52	0.60	1.24	Latch - Positive gate with preset and clear
LAPB2	8-19	2	7	0.95	1.96	0.72	1.48	0.40	0.82	0.40	0.82	Latch - Positive gate with preset and clear
LAPC1	8-21	1	5	0.81	1.67	0.70	1.44	0.74	1.52	0.61	1.26	Latch - Positive gate with clear only
LAPC2	8-23	2	6	0.96	1.98	0.72	1.48	0.41	0.84	0.40	0.82	Latch - Positive gate with clear only
LAPN1	8-25	1	4	1.06	2.18	1.08	2.22	0.73	1.50	0.57	1.17	Latch - Positive gate
LAPN2	8-27	2	5	1.27	2.62	1.24	2.55	0.40	0.82	0.36	0.74	Latch - Positive gate
LAPP1	8-29	1	5	0.72	1.48	0.53	1.09	0.74	1.52	0.58	1.19	Latch - Positive gate with preset only
LAPP2	8-31	2	6	0.93	1.92	0.59	1.22	0.34	0.70	0.32	0.66	Latch - Positive gate with preset only
LTPB1	8-33	1	13	0.82	1.69	0.75	1.54	0.75	1.54	0.61	1.26	Latch with Tri-state - Positive gate with preset and clear
LTPC1	8-36	1	12	0.82	1.69	0.75	1.54	0.75	1.54	0.61	1.26	Latch with Tri-state - Positive gate with clear only
LTPN1	8-39	1	11	0.82	1.69	0.75	1.54	0.75	1.54	0.61	1.26	Latch with Tri-state - Positive gate
LTPP1	8-42	1	12	0.82	1.69	0.75	1.54	0.75	1.54	0.61	1.26	Latch with Tri-state - Positive gate with preset only
MXH211	9-1	1	4	0.08	0.16	0.19	0.39	0.73	1.50	0.97	2.00	2 to 1 multiplexer active high gated output
MXH411	9-2	1	9	0.18	0.37	0.18	0.37	0.72	1.48	0.98	2.02	4 to 1 multiplexer active high gated output
MXL211	9-3	1	4	0.05	0.10	0.18	0.37	1.61	3.32	0.57	1.17	2 to 1 multiplexer active low gated output
MXL411	9-4	1	9	0.07	0.14	0.18	0.37	1.58	3.25	0.57	1.17	4 to 1 multiplexer active low gated output
MXN211	9-5	1	3	0.58	1.19	0.64	1.32	0.74	1.52	0.66	1.36	2 to 1 multiplexer
MXN411	9-6	1	8	1.32	2.72	1.90	3.91	1.10	2.27	0.93	1.92	4 to 1 multiplexer
MIH211	9-7	1	4	0.08	0.16	0.19	0.39	0.73	1.50	0.97	2.00	2 to 1 inverting multiplexer active high gated output
MIH411	9-8	1	8	0.18	0.37	0.16	0.33	0.72	1.48	0.99	2.04	4 to 1 inverting multiplexer active high gated output
MIL211	9-9	1	4	0.07	0.14	0.16	0.33	1.58	3.25	0.57	1.17	2 to 1 inverting multiplexer active low gated output
MIL411	9-10	1	8	0.08	0.16	0.18	0.37	1.58	3.25	0.57	1.17	4 to 1 inverting multiplexer active low gated output
MIN211	9-11	1	4	0.22	0.45	0.41	0.84	1.45	2.99	0.98	2.02	2 to 1 inverting multiplexer
MIN411	9-12	1	8	1.14	2.35	1.25	2.58	0.74	1.52	0.62	1.28	4 to 1 inverting multiplexer
DEH241	9-13	1	8	0.78	1.61	0.73	1.50	2.17	4.47	0.58	1.19	2 to 4 active high outputs decoder active High gated output
DEL241	9-14	1	8	0.89	1.83	1.02	2.10	2.13	4.39	0.59	1.22	2 to 4 active high outputs decoder active low gated output
DEN241	9-15	1	5	0.26	0.54	0.25	0.52	1.41	2.90	0.58	1.19	2 to 4 active high outputs decoder
DIH241	9-16	1	8	0.72	1.48	1.08	2.22	0.75	1.54	1.31	2.70	2 to 4 active low outputs decoder active high gated output
DIL241	9-17	1	8	0.56	1.15	0.85	1.75	0.76	1.57	1.30	2.68	2 to 4 active low outputs decoder active Low gated output
DIN241	9-18	1	5	0.53	1.09	0.47	0.97	0.76	1.57	0.93	1.92	2 to 4 active low outputs decoder
CDQY4	10-1	TYP		2.10	4.33			ps/pF	ps/pF	MAX ps/pF		Z = A. Implementation is using an inverter tree to allow high drive of clock nets while minimizing skew-
HILO	10-2	-	2									The HILO internal tie off gate is offered for managing unused inputs
BUSHOLD	10-3	-	2									Retains the value of an undriven bus
IPN	11-1	-	pad									Input pad
IPD	11-2	-	pad									Input pad with pull-down
IPU	11-3	-	pad									Input pad with pull-up
IPCBC1	11-4	1	2	0.40	0.82	0.26	0.54	0.74	1.52	0.55	1.13	CMOS level shifter
IPCBC2	11-5	2	2	0.47	0.97	0.34	0.70	0.37	0.76	0.28	0.58	CMOS level shifter
IPCBC4	11-6	4	4	0.43	0.89	0.37	0.76	0.19	0.39	0.15	0.31	CMOS level shifter
IPCBC8	11-7	8	6	0.58	1.19	0.53	1.09	0.09	0.19	0.07	0.14	CMOS level shifter
IPCIC1	11-8	1	2	0.40	0.82	0.65	1.34	0.75	1.54	0.55	1.13	Inverting CMOS level shifter
IPCIC2	11-9	2	3	0.47	0.97	0.73	1.50	0.37	0.76	0.30	0.62	Inverting CMOS level shifter
IPCIC4	11-10	4	4	0.55	1.13	0.78	1.61	0.19	0.39	0.16	0.33	Inverting CMOS level shifter
IPCIC8	11-11	8	6	0.66	1.36	1.00	2.06	0.09	0.19	0.08	0.16	Inverting CMOS level shifter
IPHBC1	11-12	1	5	0.69	1.42	0.72	1.48	0.74	1.52	0.57	1.17	CMOS level shifter with hysteresis
IPHBC2	11-13	2	5	0.73	1.50	0.77	1.59	0.38	0.78	0.32	0.66	CMOS level shifter with hysteresis

Name	Page	Drive	Cells	Timing Information								Description
				tPLH (ns)		tPHL (ns)		Δ tPLH (ns/pF)		Δ tPHL (ns/pF)		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
IPHBC4	11-14	4	6	0.82	1.69	0.89	1.83	0.21	0.43	0.20	0.41	CMOS level shifter with hysteresis
IPHBC8	11-15	8	8	1.06	2.18	1.25	2.58	0.10	0.21	0.09	0.19	CMOS level shifter with hysteresis
IPHIC1	11-16	1	5	0.83	1.71	0.95	1.96	0.75	1.54	0.55	1.13	Inverting CMOS level shifter with hysteresis
IPHIC2	11-17	2	6	0.94	1.94	1.05	2.16	0.37	0.76	0.30	0.62	Inverting CMOS level shifter with hysteresis
IPHIC4	11-18	4	7	1.01	2.08	1.07	2.20	0.19	0.39	0.16	0.33	Inverting CMOS level shifter with hysteresis
IPHIC8	11-19	8	9	1.17	2.41	1.32	2.72	0.09	0.19	0.08	0.16	Inverting CMOS level shifter with hysteresis
IPSB1	11-20	1	5	0.43	0.89	1.47	3.03	0.74	1.52	0.95	1.96	TTL level shifter with hysteresis
IPSB2	11-21	2	5	0.47	0.97	1.67	3.44	0.37	0.76	0.54	1.11	TTL level shifter with hysteresis
IPSB4	11-22	4	6	0.56	1.15	2.10	4.33	0.20	0.41	0.35	0.72	TTL level shifter with hysteresis
IPSB8	11-23	8	10	1.14	2.35	2.13	4.39	0.09	0.19	0.11	0.23	TTL level shifter with hysteresis
IPSIC1	11-24	1	5	1.46	3.01	0.72	1.48	0.74	1.52	0.88	1.81	Inverting TTL level shifter with hysteresis
IPSIC2	11-25	2	6	1.56	3.21	0.83	1.71	0.37	0.76	0.44	0.91	Inverting TTL level shifter with hysteresis
IPSIC4	11-26	4	7	1.82	3.75	0.85	1.75	0.19	0.39	0.24	0.49	Inverting TTL level shifter with hysteresis
IPSIC8	11-27	8	9	2.02	4.16	1.08	2.22	0.09	0.19	0.11	0.23	Inverting TTL level shifter with hysteresis
IPTBC1	11-28	1	2	0.26	0.54	0.69	1.42	0.75	1.54	0.90	1.85	TTL level shifter
IPTBC2	11-29	2	2	0.31	0.64	0.83	1.71	0.37	0.76	0.50	1.03	TTL level shifter
IPTBC4	11-30	4	3	0.39	0.80	1.16	2.39	0.19	0.39	0.31	0.64	TTL level shifter
IPITC1	11-31	1	2	0.72	1.48	0.56	1.15	0.74	1.52	0.85	1.75	Inverting TTL level shifter
IPITC2	11-32	2	3	0.78	1.61	0.66	1.36	0.38	0.78	0.43	0.89	Inverting TTL level shifter
IPITC4	11-33	4	4	0.96	1.98	0.69	1.42	0.20	0.41	0.23	0.47	Inverting TTL level shifter
IPITC8	11-34	8	6	1.13	2.33	0.93	1.92	0.09	0.19	0.12	0.25	Inverting TTL level shifter
VDDPAD	14-1	-	pad									VDD power pad supplies power (VDD) to the core of the array
VCCPAD	14-2	-	pad									VCC power pad supplies power (VDD) to the external I/Os
VSSPAD	14-3	-	pad									VSS power pad supplies ground to the core of the array
GNDPAD	14-4	-	pad									GND power pad supplies ground to the external I/Os
CNCT_PWR	14-5	-	none									Connects the VDD core bus with the VCC I/O bus
CNCT_GRND	14-6	-	none									Connects the VSS core bus with the GND I/O bus
COCIN	14-7	-	pad									Input part of crystal oscillator
COCO1	14-8	1	pad	2.53	5.21	1.82	3.75	0.21	0.43	0.13	0.27	Output part of crystal oscillator
COCO2	14-9	2	pad	1.27	2.62	0.99	2.04	0.10	0.21	0.07	0.14	Output part of crystal oscillator
COCO4	14-10	4	pad	0.66	1.36	0.58	1.19	0.05	0.10	0.03	0.06	Output part of crystal oscillator

Name	Page	Output Drive	Timing Information (CL = 100pF)								Description
			tPLH (ns)		tPHL (ns)		ΔtPLH (ps/pF)		ΔtPHL (ps/pF)		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
OSST02	12-1	2 mA	25.1	51.8	28.3	58.4	205	423	217	446	TTL level tri-state with slew-rate
OSST04	12-3	4 mA	13.9	28.7	16.5	34.0	103	211	109	224	TTL level tri-state with slew-rate
OSST06	12-5	6 mA	10.3	21.4	12.7	26.2	68	141	74	152	TTL level tri-state with slew-rate
OSST08	12-7	8 mA	8.73	17.9	11.0	22.7	51	106	57	117	TTL level tri-state with slew-rate
OSST12	12-9	12 mA	6.49	13.3	8.31	17.1	33	69	40	82	TTL level tri-state with slew-rate
OSST16	12-11	16 mA	5.63	11.6	7.17	14.7	25	52	32	66	TTL level tri-state with slew-rate
OSSC02	12-13	2 mA	32.2	66.3	22.5	46.4	267	550	166	342	CMOS level tri-state with slew-rate
OSSC04	12-15	4 mA	17.6	36.2	13.6	28.1	133	274	83	172	CMOS level tri-state with slew-rate
OSSC06	12-17	6 mA	13.0	26.8	10.9	22.5	89	183	57	117	CMOS level tri-state with slew-rate
OSSC08	12-19	8 mA	10.6	21.9	9.79	20.1	65	133	44	91	CMOS level tri-state with slew-rate
OSSC12	12-21	12 mA	8.04	16.5	7.41	15.2	42	87	31	65	CMOS level tri-state with slew-rate
OSSC16	12-23	16 mA	7.10	14.6	6.45	13.2	33	67	26	53	CMOS level tri-state with slew-rate
OSTT02	12-25	2 mA	24.7	50.9	27.4	56.6	205	423	217	446	TTL level totem-pole with slew-rate
OSTT04	12-26	4 mA	13.4	27.7	15.5	32.0	103	211	108	223	TTL level totem-pole with slew-rate
OSTT06	12-27	6 mA	9.86	20.3	11.7	24.1	68	141	74	151	TTL level totem-pole with slew-rate
OSTT08	12-28	8 mA	8.16	16.8	9.95	20.5	51	106	56	115	TTL level totem-pole with slew-rate
OSTT12	12-29	12 mA	6.28	12.9	7.91	16.2	33	69	40	82	TTL level totem-pole with slew-rate
OSTT16	12-30	16 mA	5.51	11.3	6.95	14.3	25	52	32	66	TTL level totem-pole with slew-rate
OSTC02	12-31	2 mA	31.7	65.4	21.6	44.6	267	550	166	342	CMOS level totem-pole with slew-rate
OSTC04	12-32	4 mA	17.0	35.2	12.6	26.0	133	274	83	171	CMOS level totem-pole with slew-rate
OSTC06	12-33	6 mA	12.4	25.7	9.82	20.2	89	183	56	115	CMOS level totem-pole with slew-rate
OSTC08	12-34	8 mA	10.0	20.6	8.53	17.5	65	133	43	89	CMOS level totem-pole with slew-rate
OSTC12	12-35	12 mA	7.80	16.0	6.95	14.3	42	87	31	64	CMOS level totem-pole with slew-rate
OSTC16	12-36	16 mA	6.97	14.3	6.20	12.7	32	67	25	52	CMOS level totem-pole with slew-rate
OSDT02	12-37	2 mA	25.2	51.9	28.2	58.2	206	424	216	444	TTL level tri-state with pull-down and slew-rate
OSDT04	12-39	4 mA	13.9	28.7	16.4	33.9	103	212	108	223	TTL level tri-state with pull-down and slew-rate
OSDT06	12-41	6 mA	10.4	21.4	12.7	26.2	68	141	74	152	TTL level tri-state with pull-down and slew-rate
OSDT08	12-43	8 mA	8.74	18.0	11.0	22.7	51	106	57	117	TTL level tri-state with pull-down and slew-rate
OSDT12	12-45	12 mA	6.49	13.3	8.30	17.1	33	69	40	82	TTL level tri-state with pull-down and slew-rate
OSDT16	12-47	16 mA	5.63	11.6	7.17	14.7	25	52	32	66	TTL level tri-state with pull-down and slew-rate
OSDC02	12-49	2 mA	32.3	66.5	22.4	46.2	268	552	165	341	CMOS level tri-state with pull-down and slew-rate
OSDC04	12-51	4 mA	17.6	36.3	13.6	28.1	133	274	83	171	CMOS level tri-state with pull-down and slew-rate
OSDC06	12-53	6 mA	13.0	26.8	10.9	22.5	89	183	56	116	CMOS level tri-state with pull-down and slew-rate
OSDC08	12-55	8 mA	10.6	21.9	9.78	20.1	65	133	44	91	CMOS level tri-state with pull-down and slew-rate
OSDC12	12-57	12 mA	8.04	16.5	7.41	15.2	42	87	31	65	CMOS level tri-state with pull-down and slew-rate
OSDC16	12-59	16 mA	7.10	14.6	6.45	13.2	33	67	26	53	CMOS level tri-state with pull-down and slew-rate
OSNT02	12-61	2 mA			27.5	56.7			220	453	TTL level N-channel open drain with slew-rate
OSNT04	12-62	4 mA			15.4	31.8			110	226	TTL level N-channel open drain with slew-rate
OSNT06	12-63	6 mA			11.5	23.7			74	151	TTL level N-channel open drain with slew-rate
OSNT08	12-64	8 mA			9.66	19.9			56	116	TTL level N-channel open drain with slew-rate
OSNT12	12-65	12 mA			7.63	15.7			40	82	TTL level N-channel open drain with slew-rate
OSNT16	12-66	16 mA			6.68	13.7			32	66	TTL level N-channel open drain with slew-rate
OSNC02	12-67	2 mA			21.5	44.3			166	342	CMOS level N-channel open drain with slew-rate
OSNC04	12-68	4 mA			12.4	25.6			83	171	CMOS level N-channel open drain with slew-rate
OSNC06	12-69	6 mA			9.49	19.5			56	115	CMOS level N-channel open drain with slew-rate
OSNC08	12-70	8 mA			8.09	16.6			43	89	CMOS level N-channel open drain with slew-rate
OSNC12	12-71	12 mA			6.51	13.4			31	64	CMOS level N-channel open drain with slew-rate
OSNC16	12-72	16 mA			5.78	11.9			25	52	CMOS level N-channel open drain with slew-rate
OSOT02	12-73	2 mA			27.5	56.8			220	453	TTL level N-channel open drain with pull-up and slew-rate

Name	Page	Output Drive	Timing Information (CL = 100pF)								Description
			tPLH (ns)		tPHL (ns)		ΔtPLH (ps/pF)		ΔtPHL (ps/pF)		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
OSOT04	12-74	4 mA			15.4	31.8			110	226	TTL level N-channel open drain with pull-up and slew-rate
OSOT06	12-75	6 mA			11.5	23.7			74	152	TTL level N-channel open drain with pull-up and slew-rate
OSOT08	12-76	8 mA			9.67	19.9			56	116	TTL level N-channel open drain with pull-up and slew-rate
OSOT12	12-77	12 mA			7.63	15.7			40	82	TTL level N-channel open drain with pull-up and slew-rate
OSOT16	12-78	16 mA			6.68	13.7			32	66	TTL level N-channel open drain with pull-up and slew-rate
OSOC02	12-79	2 mA			21.5	44.4			166	343	CMOS level N-channel open drain with pull-up and slew-rate
OSOC04	12-80	4 mA			12.4	25.6			83	171	CMOS level N-channel open drain with pull-up and slew-rate
OSOC06	12-81	6 mA			9.49	19.5			56	115	CMOS level N-channel open drain with pull-up and slew-rate
OSOC08	12-82	8 mA			8.10	16.6			43	89	CMOS level N-channel open drain with pull-up and slew-rate
OSOC12	12-83	12 mA			6.52	13.4			31	64	CMOS level N-channel open drain with pull-up and slew-rate
OSOC16	12-84	16 mA			5.78	11.9			25	52	CMOS level N-channel open drain with pull-up and slew-rate
OSPT02	12-85	2 mA	24.6	50.8			205	423			TTL level P-channel open drain with slew-rate
OSPT04	12-86	4 mA	13.3	27.5			103	211			TTL level P-channel open drain with slew-rate
OSPT06	12-87	6 mA	9.72	20.0			68	141			TTL level P-channel open drain with slew-rate
OSPT08	12-88	8 mA	7.97	16.4			51	106			TTL level P-channel open drain with slew-rate
OSPT12	12-89	12 mA	6.08	12.5			33	69			TTL level P-channel open drain with slew-rate
OSPT16	12-90	16 mA	5.31	10.9			25	52			TTL level P-channel open drain with slew-rate
OSPC02	12-91	2 mA	31.7	65.3			267	550			CMOS level P-channel open drain with slew-rate
OSPC04	12-92	4 mA	17.0	35.0			133	274			CMOS level P-channel open drain with slew-rate
OSPC06	12-93	6 mA	12.3	25.4			89	183			CMOS level P-channel open drain with slew-rate
OSPC08	12-94	8 mA	9.85	20.2			65	133			CMOS level P-channel open drain with slew-rate
OSPC12	12-95	12 mA	7.61	15.6			42	87			CMOS level P-channel open drain with slew-rate
OSPC16	12-96	16 mA	6.77	13.9			32	67			CMOS level P-channel open drain with slew-rate
OSQT02	12-97	2 mA	24.7	50.9			206	424			TTL level P-channel open drain with pull-down and slew-rate
OSQT04	12-98	4 mA	13.4	27.6			103	212			TTL level P-channel open drain with pull-down and slew-rate
OSQT06	12-99	6 mA	9.73	20.0			68	141			TTL level P-channel open drain with pull-down and slew-rate
OSQT08	12-100	8 mA	7.97	16.4			51	106			TTL level P-channel open drain with pull-down and slew-rate
OSQT12	12-101	12 mA	6.09	12.5			33	69			TTL level P-channel open drain with pull-down and slew-rate
OSQT16	12-102	16 mA	5.31	10.9			25	52			TTL level P-channel open drain with pull-down and slew-rate
OSQC02	12-103	2 mA	31.8	65.5			268	552			CMOS level P-channel open drain with pull-down and slew-rate
OSQC04	12-104	4 mA	17.0	35.0			133	274			CMOS level P-channel open drain with pull-down and slew-rate
OSQC06	12-105	6 mA	12.3	25.4			89	183			CMOS level P-channel open drain with pull-down and slew-rate
OSQC08	12-106	8 mA	9.86	20.3			65	133			CMOS level P-channel open drain with pull-down and slew-rate
OSQC12	12-107	12 mA	7.61	15.6			42	87			CMOS level P-channel open drain with pull-down and slew-rate

Name	Page	Output Drive	Timing Information (CL = 100pF)								Description
			tPLH (ns)		tPHL (ns)		ΔtPLH (ps/pF)		ΔtPHL (ps/pF)		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
OSQC16	12-108	16 mA	6.77	13.9			32	67			CMOS level P-channel open drain with pull-down and slew-rate
OSUT02	12-109	2 mA	25.0	51.5	28.4	58.5	204	420	217	447	TTL level tri-state with pull-up and slew-rate
OSUT04	12-111	4 mA	13.9	28.7	16.5	34.0	102	211	109	224	TTL level tri-state with pull-up and slew-rate
OSUT06	12-113	6 mA	10.3	21.3	12.7	26.3	68	141	74	152	TTL level tri-state with pull-up and slew-rate
OSUT08	12-115	8 mA	8.72	17.9	11.0	22.7	51	106	57	117	TTL level tri-state with pull-up and slew-rate
OSUT12	12-117	12 mA	6.49	13.3	8.31	17.1	33	69	40	82	TTL level tri-state with pull-up and slew-rate
OSUT16	12-119	16 mA	5.63	11.6	7.17	14.7	25	52	32	66	TTL level tri-state with pull-up and slew-rate
OSUC02	12-121	2 mA	32.1	66.1	22.5	46.4	266	549	166	342	CMOS level tri-state with pull-up and slew-rate
OSUC04	12-123	4 mA	17.5	36.2	13.6	28.1	133	274	83	172	CMOS level tri-state with pull-up and slew-rate
OSUC06	12-125	6 mA	13.0	26.8	10.9	22.6	89	183	57	117	CMOS level tri-state with pull-up and slew-rate
OSUC08	12-127	8 mA	10.6	21.9	9.79	20.1	65	133	44	91	CMOS level tri-state with pull-up and slew-rate
OSUC12	12-129	12 mA	8.03	16.5	7.41	15.2	42	87	31	65	CMOS level tri-state with pull-up and slew-rate
OSUC16	12-131	16 mA	7.09	14.6	6.45	13.2	33	67	26	53	CMOS level tri-state with pull-up and slew-rate
OMST12	12-133	12 mA	5.49	11.3	6.99	14.4	33	68	38	77	TTL level tri-state with moderate slew-rate
OMST16	12-135	16 mA	4.47	9.21	5.76	11.8	24	50	29	60	TTL level tri-state with moderate slew-rate
OMSC12	12-137	12 mA	6.75	13.9	6.20	12.7	42	86	29	59	CMOS level tri-state with moderate slew-rate
OMSC16	12-139	16 mA	5.61	11.5	5.15	10.6	31	65	22	46	CMOS level tri-state with moderate slew-rate
OMTT12	12-141	12 mA	5.25	10.8	6.52	13.4	33	68	37	76	TTL level totem-pole with moderate slew-rate
OMTT16	12-142	16 mA	4.09	8.43	5.05	10.4	24	50	28	58	TTL level totem-pole with moderate slew-rate
OMTC12	12-143	12 mA	6.48	13.3	5.64	11.6	42	86	29	59	CMOS level totem-pole with moderate slew-rate
OMTC16	12-144	16 mA	5.14	10.5	4.42	9.11	31	65	22	45	CMOS level totem-pole with moderate slew-rate
OMDT12	12-145	12 mA	5.49	11.3	6.99	14.4	33	68	37	77	TTL level tri-state with pull-down and moderate slew-rate
OMDT16	12-147	16 mA	4.47	9.21	5.76	11.8	24	50	29	59	TTL level tri-state with pull-down and moderate slew-rate
OMDC12	12-149	12 mA	6.75	13.9	6.20	12.7	42	86	29	59	CMOS level tri-state with pull-down and moderate slew-rate
OMDC16	12-151	16 mA	5.61	11.5	5.15	10.6	31	65	22	46	CMOS level tri-state with pull-down and moderate slew-rate
OMNT12	12-153	12 mA			6.24	12.8			37	77	TTL level N-channel open drain with moderate slew-rate
OMNT16	12-154	16 mA			4.77	9.83			28	58	TTL level N-channel open drain with moderate slew-rate
OMNC12	12-155	12 mA			5.20	10.7			28	59	CMOS level N-channel open drain with moderate slew-rate
OMNC16	12-156	16 mA			3.97	8.18			22	44	CMOS level N-channel open drain with moderate slew-rate
OMOT12	12-157	12 mA			6.24	12.8			37	77	TTL level N-channel open drain with pull-up and moderate slew-rate
OMOT16	12-158	16 mA			4.77	9.83			28	58	TTL level N-channel open drain with pull-up and moderate slew-rate
OMOC12	12-159	12 mA			5.20	10.7			28	59	CMOS level N-channel open drain with pull-up and moderate slew-rate
OMOC16	12-160	16 mA			3.97	8.18			22	44	CMOS level N-channel open drain with pull-up and moderate slew-rate
OMPT12	12-161	12 mA	5.06	10.4			33	68			TTL level P-channel open drain with moderate slew-rate
OMPT16	12-162	16 mA	3.90	8.03			24	50			TTL level P-channel open drain with moderate slew-rate
OMPC12	12-163	12 mA	6.31	13.0			42	86			CMOS level P-channel open drain with moderate slew-rate
OMPC16	12-164	16 mA	4.95	10.2			31	64			CMOS level P-channel open drain with moderate slew-rate
OMQT12	12-165	12 mA	5.06	10.4			33	68			TTL level P-channel open drain with pull-down and moderate slew-rate
OMQT16	12-166	16 mA	3.91	8.05			24	50			TTL level P-channel open drain with pull-down and moderate slew-rate
OMQC12	12-167	12 mA	6.31	13.0			42	86			CMOS level P-channel open drain with pull-down and moderate slew-rate

Name	Page	Output Drive	Timing Information (CL = 100pF)								Description
			tPLH (ns)		tPHL (ns)		Δ tPLH (ps/pF)		Δ tPHL (ps/pF)		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
OMQC16	12-168	16 mA	4.95	10.2			31	64			CMOS level P-channel open drain with pull-down and moderate slew-rate
OMUT12	12-169	12 mA	5.48	11.2	6.99	14.4	33	68	38	77	TTL level tri-state with pull-up and moderate slew-rate
OMUT16	12-171	16 mA	4.47	9.21	5.76	11.8	24	50	29	60	TTL level tri-state with pull-up and moderate slew-rate
OMUC12	12-173	12 mA	6.75	13.9	6.20	12.7	42	86	29	59	CMOS level tri-state with pull-up and moderate slew-rate
OMUC16	12-175	16 mA	5.61	11.5	5.15	10.6	31	65	23	46	CMOS level tri-state with pull-up and moderate slew-rate
ONST02	12-177	2 mA	23.9	49.3	26.1	53.9	205	423	217	446	TTL level tri-state
ONST04	12-179	4 mA	12.6	25.9	14.1	29.0	103	211	108	223	TTL level tri-state
ONST06	12-181	6 mA	8.40	17.3	9.38	19.3	68	141	73	150	TTL level tri-state
ONST08	12-183	8 mA	6.55	13.4	7.46	15.3	51	106	54	112	TTL level tri-state
ONST12	12-185	12 mA	4.43	9.13	5.19	10.6	33	68	36	75	TTL level tri-state
ONST16	12-187	16 mA	3.54	7.29	4.31	8.88	24	50	27	56	TTL level tri-state
ONSC02	12-189	2 mA	30.9	63.6	20.3	41.8	267	550	166	342	CMOS level tri-state
ONSC04	12-191	4 mA	16.0	33.1	11.2	23.1	133	274	83	171	CMOS level tri-state
ONSC06	12-193	6 mA	10.7	22.1	7.48	15.4	89	183	55	113	CMOS level tri-state
ONSC08	12-195	8 mA	8.09	16.6	6.08	12.5	64	133	41	85	CMOS level tri-state
ONSC12	12-197	12 mA	5.47	11.2	4.29	8.84	42	86	28	57	CMOS level tri-state
ONSC16	12-199	16 mA	4.43	9.13	3.69	7.60	31	64	21	43	CMOS level tri-state
ONTT02	12-201	2 mA	23.5	48.4	25.3	52.2	205	423	217	446	TTL level totem-pole
ONTT04	12-202	4 mA	11.8	24.4	12.8	26.3	103	211	108	223	TTL level totem-pole
ONTT06	12-203	6 mA	8.10	16.6	8.79	18.1	68	141	73	150	TTL level totem-pole
ONTT08	12-204	8 mA	6.16	12.6	6.70	13.8	51	106	54	112	TTL level totem-pole
ONTT12	12-205	12 mA	4.13	8.51	4.68	9.64	33	68	36	75	TTL level totem-pole
ONTT16	12-206	16 mA	3.22	6.63	3.77	7.77	24	50	27	56	TTL level totem-pole
ONTC02	12-207	2 mA	30.4	62.6	19.5	40.2	267	550	166	342	CMOS level totem-pole
ONTC04	12-208	4 mA	15.2	31.5	9.91	20.4	133	274	83	171	CMOS level totem-pole
ONTC06	12-209	6 mA	10.4	21.4	6.88	14.1	89	183	55	113	CMOS level totem-pole
ONTC08	12-210	8 mA	7.65	15.7	5.30	10.9	64	133	41	85	CMOS level totem-pole
ONTC12	12-211	12 mA	5.11	10.5	3.79	7.81	42	86	27	57	CMOS level totem-pole
ONTC16	12-212	16 mA	4.01	8.26	3.16	6.51	31	64	21	42	CMOS level totem-pole
ONDT02	12-213	2 mA	24.0	49.4	26.0	53.6	206	424	216	444	TTL level tri-state with pull-down
ONDT04	12-215	4 mA	12.6	26.0	14.0	29.0	103	212	108	223	TTL level tri-state with pull-down
ONDT06	12-217	6 mA	8.42	17.3	9.37	19.3	68	141	73	149	TTL level tri-state with pull-down
ONDT08	12-219	8 mA	6.56	13.5	7.45	15.3	51	106	54	112	TTL level tri-state with pull-down
ONDT12	12-221	12 mA	4.43	9.13	5.19	10.6	33	68	36	75	TTL level tri-state with pull-down
ONDT16	12-223	16 mA	3.54	7.29	4.31	8.88	24	50	27	56	TTL level tri-state with pull-down
ONDC02	12-225	2 mA	31.0	63.8	20.2	41.6	268	552	165	340	CMOS level tri-state with pull-down
ONDC04	12-227	4 mA	16.1	33.1	11.2	23.0	133	274	83	170	CMOS level tri-state with pull-down
ONDC06	12-229	6 mA	10.7	22.1	7.47	15.3	89	183	55	113	CMOS level tri-state with pull-down
ONDC08	12-231	8 mA	8.11	16.7	6.08	12.5	64	133	41	85	CMOS level tri-state with pull-down
ONDC12	12-233	12 mA	5.47	11.2	4.29	8.84	42	86	28	57	CMOS level tri-state with pull-down
ONDC16	12-235	16 mA	4.43	9.13	3.69	7.60	31	64	21	43	CMOS level tri-state with pull-down
ONNT02	12-237	2 mA			25.4	52.3			220	452	TTL level N-channel open drain
ONNT04	12-238	4 mA			12.7	26.3			110	226	TTL level N-channel open drain
ONNT06	12-239	6 mA			8.69	17.9			73	150	TTL level N-channel open drain
ONNT08	12-240	8 mA			6.61	13.6			55	112	TTL level N-channel open drain
ONNT12	12-241	12 mA			4.55	9.37			36	75	TTL level N-channel open drain
ONNT16	12-242	16 mA			3.57	7.35			27	56	TTL level N-channel open drain
ONNC02	12-243	2 mA			19.4	40.0			166	342	CMOS level N-channel open drain

Name	Page	Output Drive	Timing Information (CL = 100pF)								Description
			tPLH (ns)		tPHL (ns)		ΔtPLH (ps/pF)		ΔtPHL (ps/pF)		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
ONNC04	12-244	4 mA			9.81	20.2			83	171	CMOS level N-channel open drain
ONNC06	12-245	6 mA			6.71	13.8			55	113	CMOS level N-channel open drain
ONNC08	12-246	8 mA			5.12	10.5			41	85	CMOS level N-channel open drain
ONNC12	12-247	12 mA			3.56	7.33			27	57	CMOS level N-channel open drain
ONNC16	12-248	16 mA			2.83	5.83			21	42	CMOS level N-channel open drain
ONOT02	12-249	2 mA			25.4	52.4					TTL level N-channel open drain with pull-up
ONOT04	12-250	4 mA			12.8	26.3			110	226	TTL level N-channel open drain with pull-up
ONOT06	12-251	6 mA			8.70	17.9			73	150	TTL level N-channel open drain with pull-up
ONOT08	12-252	8 mA			6.61	13.6			55	112	TTL level N-channel open drain with pull-up
ONOT12	12-253	12 mA			4.55	9.37			36	75	TTL level N-channel open drain with pull-up
ONOT16	12-254	16 mA			3.57	7.35			27	56	TTL level N-channel open drain with pull-up
ONOC02	12-255	2 mA			19.4	40.0			166	343	CMOS level N-channel open drain with pull-up
ONOC04	12-256	4 mA			9.81	20.2			83	171	CMOS level N-channel open drain with pull-up
ONOC06	12-257	6 mA			6.71	13.8			55	113	CMOS level N-channel open drain with pull-up
ONOC08	12-258	8 mA			5.12	10.5			41	85	CMOS level N-channel open drain with pull-up
ONOC12	12-259	12 mA			3.56	7.33			27	57	CMOS level N-channel open drain with pull-up
ONOC16	12-260	16 mA			2.83	5.83			21	42	CMOS level N-channel open drain with pull-up
ONPT02	12-261	2 mA	23.4	48.2			205	423			TTL level P-channel open drain
ONPT04	12-262	4 mA	11.8	24.3			103	211			TTL level P-channel open drain
ONPT06	12-263	6 mA	8.01	16.5			68	141			TTL level P-channel open drain
ONPT08	12-264	8 mA	6.07	12.5			51	106			TTL level P-channel open drain
ONPT12	12-265	12 mA	4.02	8.28			33	68			TTL level P-channel open drain
ONPT16	12-266	16 mA	3.08	6.34			24	50			TTL level P-channel open drain
ONPC02	12-267	2 mA	30.3	62.5			267	550			CMOS level P-channel open drain
ONPC04	12-268	4 mA	15.2	31.3			133	274			CMOS level P-channel open drain
ONPC06	12-269	6 mA	10.3	21.2			89	183			CMOS level P-channel open drain
ONPC08	12-270	8 mA	7.55	15.5			64	133			CMOS level P-channel open drain
ONPC12	12-271	12 mA	5.01	10.3			42	86			CMOS level P-channel open drain
ONPC16	12-272	16 mA	3.89	8.01			31	64			CMOS level P-channel open drain
ONQT02	12-273	2 mA	23.5	48.4			206	424			TTL level P-channel open drain with pull-down
ONQT04	12-274	4 mA	11.8	24.3			103	212			TTL level P-channel open drain with pull-down
ONQT06	12-275	6 mA	8.01	16.5			68	141			TTL level P-channel open drain with pull-down
ONQT08	12-276	8 mA	6.07	12.5			51	106			TTL level P-channel open drain with pull-down
ONQT12	12-277	12 mA	4.02	8.28			33	68			TTL level P-channel open drain with pull-down
ONQT16	12-278	16 mA	3.08	6.34			24	50			TTL level P-channel open drain with pull-down
ONQC02	12-279	2 mA	30.4	62.7			268	552			CMOS level P-channel open drain with pull-down
ONQC04	12-280	4 mA	15.2	31.3			133	274			CMOS level P-channel open drain with pull-down
ONQC06	12-281	6 mA	10.3	21.2			89	183			CMOS level P-channel open drain with pull-down
ONQC08	12-282	8 mA	7.56	15.5			64	133			CMOS level P-channel open drain with pull-down
ONQC12	12-283	12 mA	5.01	10.3			42	86			CMOS level P-channel open drain with pull-down
ONQC16	12-284	16 mA	3.89	8.01			31	64			CMOS level P-channel open drain with pull-down
ONUT02	12-285	2 mA	23.8	49.0	26.2	53.9	204	420	217	447	TTL level tri-state with pull-up
ONUT04	12-287	4 mA	12.5	25.8	14.1	29.0	102	211	108	223	TTL level tri-state with pull-up
ONUT06	12-289	6 mA	8.39	17.2	9.38	19.3	68	141	73	150	TTL level tri-state with pull-up
ONUT08	12-291	8 mA	6.55	13.4	7.46	15.3	51	106	54	112	TTL level tri-state with pull-up
ONUT12	12-293	12 mA	4.42	9.11	5.19	10.6	33	68	36	75	TTL level tri-state with pull-up
ONUT16	12-295	16 mA	3.54	7.29	4.31	8.88	24	50	27	56	TTL level tri-state with pull-up
ONUC02	12-297	2 mA	30.8	63.4	20.3	41.9	266	549	166	342	CMOS level tri-state with pull-up
ONUC04	12-299	4 mA	16.0	33.0	11.2	23.1	133	274	83	171	CMOS level tri-state with pull-up

Name	Page	Output Drive	Timing Information (CL = 100pF)								Description
			tPLH (ns)		tPHL (ns)		ΔtPLH (ps/pF)		ΔtPHL (ps/pF)		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
ONUC06	12-301	6 mA	10.7	22.1	7.49	15.4	89	183	55	113	CMOS level tri-state with pull-up
ONUC08	12-303	8 mA	8.09	16.6	6.09	12.5	64	132	41	85	CMOS level tri-state with pull-up
ONUC12	12-305	12 mA	5.47	11.2	4.29	8.84	42	86	28	57	CMOS level tri-state with pull-up
ONUC16	12-307	16 mA	4.43	9.13	3.69	7.60	31	64	21	43	CMOS level tri-state with pull-up
BSTTD02	13-1	2 mA	25.2	51.9	28.2	58.2	206	424	216	444	Bidirectional TTL output with pull-down. Output drive is 2 mA with slew-rate
BSTTD04	13-3	4 mA	13.9	28.7	16.4	33.9	103	212	108	223	Bidirectional TTL output with pull-down. Output drive is 4 mA with slew-rate
BSTTD06	13-5	6 mA	10.4	21.4	12.7	26.2	68	141	74	152	Bidirectional TTL output with pull-down. Output drive is 6 mA with slew-rate
BSTTD08	13-7	8 mA	8.74	18.0	11.0	22.7	51	106	57	117	Bidirectional TTL output with pull-down. Output drive is 8 mA with slew-rate
BSTTD12	13-9	12 mA	6.49	13.3	8.30	17.1	33	69	40	82	Bidirectional TTL output with pull-down. Output drive is 12 mA with slew-rate
BSTTD16	13-11	16 mA	5.63	11.6	7.17	14.7	25	52	32	66	Bidirectional TTL output with pull-down. Output drive is 16 mA with slew-rate
BSTTN02	13-13	2 mA	25.1	51.8	28.3	58.4	205	423	217	446	Bidirectional TTL output. Output drive is 2 mA with slew-rate
BSTTN04	13-15	4 mA	13.9	28.7	16.5	34.0	103	211	109	224	Bidirectional TTL output. Output drive is 4 mA with slew-rate
BSTTN06	13-17	6 mA	10.3	21.4	12.7	26.2	68	141	74	152	Bidirectional TTL output. Output drive is 6 mA with slew-rate
BSTTN08	13-19	8 mA	8.73	17.9	11.0	22.7	51	106	57	117	Bidirectional TTL output. Output drive is 8 mA with slew-rate
BSTTN12	13-21	12 mA	6.49	13.3	8.31	17.1	33	69	40	82	Bidirectional TTL output. Output drive is 12 mA with slew-rate
BSTTN16	13-23	16 mA	5.63	11.6	7.17	14.7	25	52	32	66	Bidirectional TTL output. Output drive is 16 mA with slew-rate
BSTTU02	13-25	2 mA	25.0	51.5	28.4	58.5	204	420	217	447	Bidirectional TTL output with pull-up. Output drive is 2 mA with slew-rate
BSTTU04	13-27	4 mA	13.9	28.7	16.5	34.0	102	211	109	224	Bidirectional TTL output with pull-up. Output drive is 4 mA with slew-rate
BSTTU06	13-29	6 mA	10.3	21.3	12.7	26.3	68	141	74	152	Bidirectional TTL output with pull-up. Output drive is 6 mA with slew-rate
BSTTU08	13-31	8 mA	8.72	17.9	11.0	22.7	51	106	57	117	Bidirectional TTL output with pull-up. Output drive is 8 mA with slew-rate
BSTTU12	13-33	12 mA	6.49	13.3	8.31	17.1	33	69	40	82	Bidirectional TTL output with pull-up. Output drive is 12 mA with slew-rate
BSTTU16	13-35	16 mA	5.63	11.6	7.17	14.7	25	52	32	66	Bidirectional TTL output with pull-up. Output drive is 16 mA with slew-rate
BSTCD02	13-37	2 mA	32.3	66.5	22.4	46.2	268	552	165	341	Bidirectional CMOS output with pull-down. Output drive is 2 mA with slew-rate
BSTCD04	13-39	4 mA	17.6	36.3	13.6	28.1	133	274	83	171	Bidirectional CMOS output with pull-down. Output drive is 4 mA with slew-rate
BSTCD06	13-41	6 mA	13.0	26.8	10.9	22.5	89	183	56	116	Bidirectional CMOS output with pull-down. Output drive is 6 mA with slew-rate
BSTCD08	13-43	8 mA	10.6	21.9	9.78	20.1	65	133	44	91	Bidirectional CMOS output with pull-down. Output drive is 8 mA with slew-rate
BSTCD12	13-45	12 mA	8.04	16.5	7.41	15.2	42	87	31	65	Bidirectional CMOS output with pull-down. Output drive is 12 mA with slew-rate
BSTCD16	13-47	16 mA	7.10	14.6	6.45	13.2	33	67	26	53	Bidirectional CMOS output with pull-down. Output drive is 16 mA with slew-rate

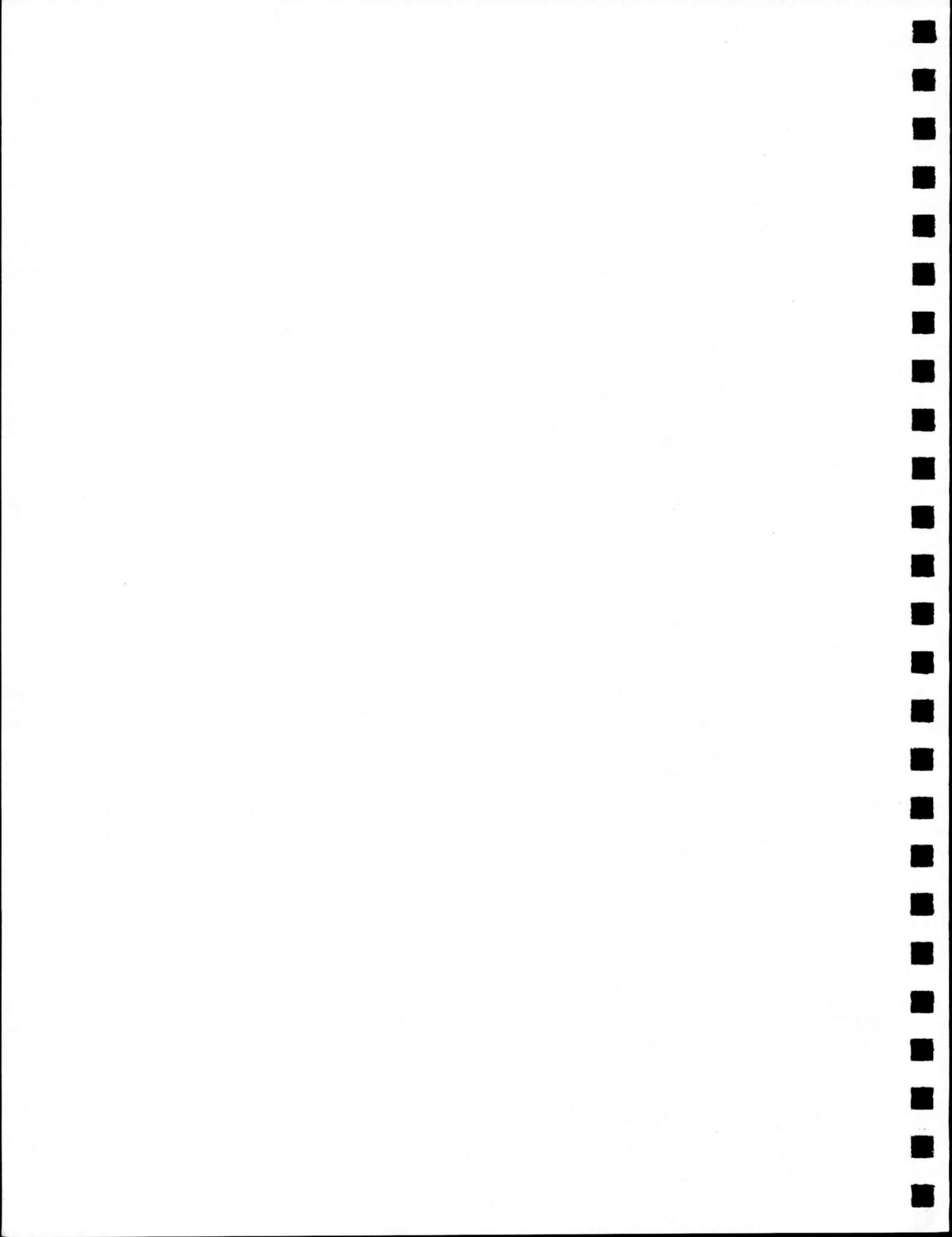
Name	Page	Output Drive	Timing Information (CL = 100pF)								Description
			tPLH (ns)		tPHL (ns)		ΔtPLH (ps/pF)		ΔtPHL (ps/pF)		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
BSTCN02	13-49	2 mA	32.2	66.3	22.5	46.4	267	550	166	342	Bidirectional CMOS output. Output drive is 2 mA with slew-rate
BSTCN04	13-51	4 mA	17.6	36.2	13.6	28.1	133	274	83	172	Bidirectional CMOS output. Output drive is 4 mA with slew-rate
BSTCN06	13-53	6 mA	13.0	26.8	10.9	22.5	89	183	57	117	Bidirectional CMOS output. Output drive is 6 mA with slew-rate
BSTCN08	13-55	8 mA	10.6	21.9	9.79	20.1	65	133	44	91	Bidirectional CMOS output. Output drive is 8 mA with slew-rate
BSTCN12	13-57	12 mA	8.04	16.5	7.41	15.2	42	87	31	65	Bidirectional CMOS output. Output drive is 12 mA with slew-rate
BSTCN16	13-59	16 mA	7.10	14.6	6.45	13.2	33	67	26	53	Bidirectional CMOS output. Output drive is 16 mA with slew-rate
BSTCU02	13-61	2 mA	32.1	66.1	22.5	46.4	266	549	166	342	Bidirectional CMOS output with pull-up. Output drive is 2 mA with slew-rate
BSTCU04	13-63	4 mA	17.5	36.2	13.6	28.1	133	274	83	172	Bidirectional CMOS output with pull-up. Output drive is 4 mA with slew-rate
BSTCU06	13-65	6 mA	13.0	26.8	10.9	22.6	89	183	57	117	Bidirectional CMOS output with pull-up. Output drive is 6 mA with slew-rate
BSTCU08	13-67	8 mA	10.6	21.9	9.79	20.1	65	133	44	91	Bidirectional CMOS output with pull-up. Output drive is 8 mA with slew-rate
BSTCU12	13-69	12 mA	8.03	16.5	7.41	15.2	42	87	31	65	Bidirectional CMOS output with pull-up. Output drive is 12 mA with slew-rate
BSTCU16	13-71	16 mA	7.09	14.6	6.45	13.2	33	67	26	53	Bidirectional CMOS output with pull-up. Output drive is 16 mA with slew-rate
BSNTU02	13-73	2 mA			27.5	56.8			220	453	N-channel open drain bidirectional TTL output with pull-up. Output drive is 2 mA with slew-rate
BSNTU04	13-74	4 mA			15.4	31.8			110	226	N-channel open drain bidirectional TTL output with pull-up. Output drive is 4 mA with slew-rate
BSNTU06	13-75	6 mA			11.5	23.7			74	152	N-channel open drain bidirectional TTL output with pull-up. Output drive is 6 mA with slew-rate
BSNTU08	13-76	8 mA			9.67	19.9			56	116	N-channel open drain bidirectional TTL output with pull-up. Output drive is 8 mA with slew-rate
BSNTU12	13-77	12 mA			7.63	15.7			40	82	N-channel open drain bidirectional TTL output with pull-up. Output drive is 12 mA with slew-rate
BSNTU16	13-78	16 mA			6.68	13.7			32	66	N-channel open drain bidirectional TTL output with pull-up. Output drive is 16 mA with slew-rate
BSNCU02	13-79	2 mA			21.5	44.4			166	343	N-channel open drain bidirectional CMOS output with pull-up. Output drive is 2 mA with slew-rate
BSNCU04	13-80	4 mA			12.4	25.6			83	171	N-channel open drain bidirectional CMOS output with pull-up. Output drive is 4 mA with slew-rate
BSNCU06	13-81	6 mA			9.49	19.5			56	115	N-channel open drain bidirectional CMOS output with pull-up. Output drive is 6 mA with slew-rate
BSNCU08	13-82	8 mA			8.10	16.6			43	89	N-channel open drain bidirectional CMOS output with pull-up. Output drive is 8 mA with slew-rate
BSNCU12	13-83	12 mA			6.52	13.4			31	64	N-channel open drain bidirectional CMOS output with pull-up. Output drive is 12 mA with slew-rate
BSNCU16	13-84	16 mA			5.78	11.9			25	52	N-channel open drain bidirectional CMOS output with pull-up. Output drive is 16 mA with slew-rate
BSPTD02	13-85	2 mA	24.7	50.9			206	424			P-channel open drain bidirectional TTL output with pull-down. Output drive is 2 mA with slew-rate
BSPTD04	13-86	4 mA	13.4	27.6			103	212			P-channel open drain bidirectional TTL output with pull-down. Output drive is 4 mA with slew-rate

Name	Page	Output Drive	Timing Information (CL = 100pF)								Description
			tPLH (ns)		tPHL (ns)		ΔtPLH (ps/pF)		ΔtPHL (ps/pF)		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
BSPTD06	13-87	6 mA	9.73	20.0			68	141			P-channel open drain bidirectional TTL output with pull-down. Output drive is 6 mA with slew-rate
BSPTD08	13-88	8 mA	7.97	16.4			51	106			P-channel open drain bidirectional TTL output with pull-down. Output drive is 8 mA with slew-rate
BSPTD12	13-89	12 mA	6.09	12.5			33	69			P-channel open drain bidirectional TTL output with pull-down. Output drive is 12 mA with slew-rate
BSPTD16	13-90	16 mA	5.31	10.9			25	52			P-channel open drain bidirectional TTL output with pull-down. Output drive is 16 mA with slew-rate
BSPCD02	13-91	2 mA	31.8	65.5			268	552			P-channel open drain bidirectional CMOS output with pull-down. Output drive is 2 mA with slew-rate
BSPCD04	13-92	4 mA	17.0	35.0			133	274			P-channel open drain bidirectional CMOS output with pull-down. Output drive is 4 mA with slew-rate
BSPCD06	13-93	6 mA	12.3	25.4			89	183			P-channel open drain bidirectional CMOS output with pull-down. Output drive is 6 mA with slew-rate
BSPCD08	13-94	8 mA	9.86	20.3			65	133			P-channel open drain bidirectional CMOS output with pull-down. Output drive is 8 mA with slew-rate
BSPCD12	13-95	12 mA	7.61	15.6			42	87			P-channel open drain bidirectional CMOS output with pull-down. Output drive is 12 mA with slew-rate
BSPCD16	13-96	16 mA	6.77	13.9			32	67			P-channel open drain bidirectional CMOS output with pull-down. Output drive is 16 mA with slew-rate
BMTTD12	13-97	12 mA	5.49	11.3	6.99	14.4	33	68	37	77	Bidirectional TTL output with pull-down. Output drive is 12 mA with moderate slew-rate
BMTTD16	13-99	16 mA	4.47	9.21	5.76	11.8	24	50	29	59	Bidirectional TTL output with pull-down. Output drive is 16 mA with moderate slew-rate
BMTTN12	13-101	12 mA	5.49	11.3	6.99	14.4	33	68	38	77	Bidirectional TTL output. Output drive is 12 mA with moderate slew-rate
BMTTN16	13-103	16 mA	4.47	9.21	5.76	11.8	24	50	29	60	Bidirectional TTL output. Output drive is 16 mA with moderate slew-rate
BMTTU12	13-105	12 mA	5.48	11.2	6.99	14.4	33	68	38	77	Bidirectional TTL output with pull-up. Output drive is 12 mA with moderate slew-rate
BMTTU16	13-107	16 mA	4.47	9.21	5.76	11.8	24	50	29	60	Bidirectional TTL output with pull-up. Output drive is 16 mA with moderate slew-rate
BMTCD12	13-109	12 mA	6.75	13.9	6.20	12.7	42	86	29	59	Bidirectional CMOS output with pull-down. Output drive is 12 mA with moderate slew-rate
BMTCD16	13-111	16 mA	5.61	11.5	5.15	10.6	31	65	22	46	Bidirectional CMOS output with pull-down. Output drive is 16 mA with moderate slew-rate
BMTCN12	13-113	12 mA	6.75	13.9	6.20	12.7	42	86	29	59	Bidirectional CMOS output. Output drive is 12 mA with moderate slew-rate
BMTCN16	13-115	16 mA	5.61	11.5	5.15	10.6	31	65	22	46	Bidirectional CMOS output. Output drive is 16 mA with moderate slew-rate
BMTCU12	13-117	12 mA	6.75	13.9	6.20	12.7	42	86	29	59	Bidirectional CMOS output with pull-up. Output drive is 12 mA with moderate slew-rate
BMTCU16	13-119	16 mA	5.61	11.5	5.15	10.6	31	65	23	46	Bidirectional CMOS output with pull-up. Output drive is 16 mA with moderate slew-rate
BMNTU12	13-121	-		6.24	12.8				37	77	PARAMETER
BMNTU16	13-122	-		4.77	9.83				28	58	PARAMETER
BMNCU12	13-123	-		5.20	10.7				28	59	PARAMETER
BMNCU16	13-124	-		3.97	8.18				22	44	PARAMETER
BMPTD12	13-125	12 mA	5.06	10.4			33	68			P-channel open drain bidirectional TTL output with pull-down. Output drive is 12 mA with moderate slew-rate
BMPTD16	13-126	16 mA	3.91	8.05			24	50			P-channel open drain bidirectional TTL output with pull-down. Output drive is 16 mA with moderate slew-rate
BMPCD12	13-127	-	6.31	13.0			42	86			PARAMETER

Name	Page	Output Drive	Timing Information (CL = 100pF)								Description
			tPLH (ns)		tPHL (ns)		ΔtPLH (ps/pF)		ΔtPHL (ps/pF)		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
BMPCD16	13-128	16 mA	4.95	10.2			31	64			P-channel open drain bidirectional CMOS output with pull-down. Output drive is 16 mA with moderate slew-rate
BNTTD02	13-129	2 mA	24.0	49.4	26.0	53.6	206	424	216	444	Bidirectional TTL output with pull-down. Output drive is 2 mA
BNTTD04	13-131	4 mA	12.6	26.0	14.0	29.0	103	212	108	223	Bidirectional TTL output with pull-down. Output drive is 4 mA
BNTTD06	13-133	6 mA	8.42	17.3	9.37	19.3	68	141	73	149	Bidirectional TTL output with pull-down. Output drive is 6 mA
BNTTD08	13-135	8 mA	6.56	13.5	7.45	15.3	51	106	54	112	Bidirectional TTL output with pull-down. Output drive is 8 mA
BNTTD12	13-137	12 mA	4.43	9.13	5.19	10.6	33	68	36	75	Bidirectional TTL output with pull-down. Output drive is 12 mA
BNTTD16	13-139	16 mA	3.54	7.29	4.31	8.88	24	50	27	56	Bidirectional TTL output with pull-down. Output drive is 16 mA
BNTTN02	13-141	2 mA	23.9	49.3	26.1	53.9	205	423	217	446	Bidirectional TTL output. Output drive is 2 mA
BNTTN04	13-143	4 mA	12.6	25.9	14.1	29.0	103	211	108	223	Bidirectional TTL output. Output drive is 4 mA
BNTTN06	13-145	6 mA	8.40	17.3	9.38	19.3	68	141	73	150	Bidirectional TTL output. Output drive is 6 mA
BNTTN08	13-147	8 mA	6.55	13.4	7.46	15.3	51	106	54	112	Bidirectional TTL output. Output drive is 8 mA
BNTTN12	13-149	12 mA	4.43	9.13	5.19	10.6	33	68	36	75	Bidirectional TTL output. Output drive is 12 mA
BNTTN16	13-151	16 mA	3.54	7.29	4.31	8.88	24	50	27	56	Bidirectional TTL output. Output drive is 16 mA
BNTTU02	13-153	2 mA	23.8	49.0	26.2	53.9	204	420	217	447	Bidirectional TTL output with pull-up. Output drive is 2 mA
BNTTU04	13-155	4 mA	12.5	25.8	14.1	29.0	102	211	108	223	Bidirectional TTL output with pull-up. Output drive is 4 mA
BNTTU06	13-157	6 mA	8.39	17.2	9.38	19.3	68	141	73	150	Bidirectional TTL output with pull-up. Output drive is 6 mA
BNTTU08	13-159	8 mA	6.55	13.4	7.46	15.3	51	106	54	112	Bidirectional TTL output with pull-up. Output drive is 8 mA
BNTTU12	13-161	12 mA	4.42	9.11	5.19	10.6	33	68	36	75	Bidirectional TTL output with pull-up. Output drive is 12 mA
BNTTU16	13-163	16 mA	3.54	7.29	4.31	8.88	24	50	27	56	Bidirectional TTL output with pull-up. Output drive is 16 mA
BNTCD02	13-165	2 mA	31.0	63.8	20.2	41.6	268	552	165	340	Bidirectional CMOS output with pull-down. Output drive is 2 mA
BNTCD04	13-167	4 mA	16.1	33.1	11.2	23.0	133	274	83	170	Bidirectional CMOS output with pull-down. Output drive is 4 mA
BNTCD06	13-169	6 mA	10.7	22.1	7.47	15.3	89	183	55	113	Bidirectional CMOS output with pull-down. Output drive is 6 mA
BNTCD08	13-171	8 mA	8.11	16.7	6.08	12.5	64	133	41	85	Bidirectional CMOS output with pull-down. Output drive is 8 mA
BNTCD12	13-173	12 mA	5.47	11.2	4.29	8.84	42	86	28	57	Bidirectional CMOS output with pull-down. Output drive is 12 mA
BNTCD16	13-175	16 mA	4.43	9.13	3.69	7.60	31	64	21	43	Bidirectional CMOS output with pull-down. Output drive is 16 mA
BNTCN02	13-177	2 mA	30.9	63.6	20.3	41.8	267	550	166	342	Bidirectional CMOS output. Output drive is 2 mA
BNTCN04	13-179	4 mA	16.0	33.1	11.2	23.1	133	274	83	171	Bidirectional CMOS output. Output drive is 4 mA
BNTCN06	13-181	6 mA	10.7	22.1	7.48	15.4	89	183	55	113	Bidirectional CMOS output. Output drive is 6 mA
BNTCN08	13-183	8 mA	8.09	16.6	6.08	12.5	64	133	41	85	Bidirectional CMOS output. Output drive is 8 mA
BNTCN12	13-185	12 mA	5.47	11.2	4.29	8.84	42	86	28	57	Bidirectional CMOS output. Output drive is 12 mA
BNTCN16	13-187	16 mA	4.43	9.13	3.69	7.60	31	64	21	43	Bidirectional CMOS output. Output drive is 16 mA
BNTCU02	13-189	2 mA	30.8	63.4	20.3	41.9	266	549	166	342	Bidirectional CMOS output with pull-up. Output drive is 2 mA
BNTCU04	13-191	4 mA	16.0	33.0	11.2	23.1	133	274	83	171	Bidirectional CMOS output with pull-up. Output drive is 4 mA
BNTCU06	13-193	6 mA	10.7	22.1	7.49	15.4	89	183	55	113	Bidirectional CMOS output with pull-up. Output drive is 6 mA

Name	Page	Output Drive	Timing Information (CL = 100pF)								Description	
			tPLH (ns)		tPHL (ns)		ΔtPLH (ps/pF)		ΔtPHL (ps/pF)			
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX		
BNTCU08	13-195	8 mA	8.09	16.6	6.09	12.5	64	132	41	85	Bidirectional CMOS output with pull-up. Output drive is 8 mA	
BNTCU12	13-197	12 mA	5.47	11.2	4.29	8.84	42	86	28	57	Bidirectional CMOS output with pull-up. Output drive is 12 mA	
BNTCU16	13-199	16 mA	4.43	9.13	3.69	7.60	31	64	21	43	Bidirectional CMOS output with pull-up. Output drive is 16 mA	
BNNTU02	13-201	2 mA			25.4	52.4					N-channel open drain bidirectional TTL output with pull-up. Output drive is 2 mA	
BNNTU04	13-202	4 mA			12.8	26.3				110	226	N-channel open drain bidirectional TTL output with pull-up. Output drive is 4 mA
BNNTU06	13-203	6 mA			8.70	17.9				73	150	N-channel open drain bidirectional TTL output with pull-up. Output drive is 6 mA
BNNTU08	13-204	8 mA			6.61	13.6				55	112	N-channel open drain bidirectional TTL output with pull-up. Output drive is 8 mA
BNNTU12	13-205	12 mA			4.55	9.37				36	75	N-channel open drain bidirectional TTL output with pull-up. Output drive is 12 mA
BNNTU16	13-206	16 mA			3.57	7.35				27	56	N-channel open drain bidirectional TTL output with pull-up. Output drive is 16 mA
BNNCU02	13-207	2 mA			19.4	40.0				166	343	N-channel open drain bidirectional CMOS output with pull-up. Output drive is 2 mA
BNNCU04	13-208	4 mA			9.81	20.2				83	171	N-channel open drain bidirectional CMOS output with pull-up. Output drive is 4 mA
BNNCU06	13-209	6 mA			6.71	13.8				55	113	N-channel open drain bidirectional CMOS output with pull-up. Output drive is 6 mA
BNNCU08	13-210	8 mA			5.12	10.5				41	85	N-channel open drain bidirectional CMOS output with pull-up. Output drive is 8 mA
BNNCU12	13-211	12 mA			3.56	7.33				27	57	N-channel open drain bidirectional CMOS output with pull-up. Output drive is 12 mA
BNNCU16	13-212	16 mA			2.83	5.83				21	42	N-channel open drain bidirectional CMOS output with pull-up. Output drive is 16 mA
BNPTD02	13-213	2 mA	23.5	48.4			206	424				P-channel open drain bidirectional TTL output with pull-down. Output drive is 2 mA
BNPTD04	13-214	4 mA	11.8	24.3			103	212				P-channel open drain bidirectional TTL output with pull-down. Output drive is 4 mA
BNPTD06	13-215	6 mA	8.01	16.5			68	141				P-channel open drain bidirectional TTL output with pull-down. Output drive is 6 mA
BNPTD08	13-216	8 mA	6.07	12.5			51	106				P-channel open drain bidirectional TTL output with pull-down. Output drive is 8 mA
BNPTD12	13-217	12 mA	4.02	8.28			33	68				P-channel open drain bidirectional TTL output with pull-down. Output drive is 12 mA
BNPTD16	13-218	16 mA	3.08	6.34			24	50				P-channel open drain bidirectional TTL output with pull-down. Output drive is 16 mA
BNPCD02	13-219	2 mA	30.4	62.7			268	552				P-channel open drain bidirectional CMOS output with pull-down. Output drive is 2 mA
BNPCD04	13-220	4 mA	15.2	31.3			133	274				P-channel open drain bidirectional CMOS output with pull-down. Output drive is 4 mA
BNPCD06	13-221	6 mA	10.3	21.2			89	183				P-channel open drain bidirectional CMOS output with pull-down. Output drive is 6 mA
BNPCD08	13-222	8 mA	7.56	15.5			64	133				P-channel open drain bidirectional CMOS output with pull-down. Output drive is 8 mA
BNPCD12	13-223	12 mA	5.01	10.3			42	86				P-channel open drain bidirectional CMOS output with pull-down. Output drive is 12 mA

Name	Page	Output Drive	Timing Information (CL = 100pF)								Description
			tPLH (ns)		tPHL (ns)		Δ tPLH (ps/pF)		Δ tPHL (ps/pF)		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
BNPCD16	13-224	16 mA	3.89	8.01			31	64			P-channel open drain bidirectional CMOS output with pull-down. Output drive is 16 mA



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Fax: (301) 384-9596

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182 Main Street
Salem, NH 03079
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Fax: (603) 898-6895

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Burtonsville, MD 20866
Tel: (301) 236-0530
Fax: (301) 384-9596

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8316 1254th Avenue N.E.
Redmond, WA 98052
Tel: (206)-885-5064
Fax: (206) 885-2262

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Fax: (414) 646-3243

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Fax: 61-2-638-1789

Mr. Bob Roughton, Marketing Manager

CANADA

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Don Didonato

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Europe and Middle East Headquarters

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Fax: 972-4-855-1122

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Tel: 852-2303-0711

Fax: 852-2376-3360

Mr. Mandie Chong, Marketing Director

INDIA

CHIP EXPRESS CORPORATION

Josh Bellin

2903 Bunker Hill Lane Suite 105

Santa Clara, CA 95054

USA

Tel: 408-988-2445 x176

Fax: 408-988-2449

email: joshb@chipx.com

ISRAEL

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Herzlia, ISRAEL 46305

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154-17 Samsung-Dong Kangnam-Ku
Seoul, KOREA 135-090
Tel: 82-2-3450-7117
Fax: 82-2-553-2998 or 2109
Mr. K.Y. Lee, Senior manager, Sales

LATIN AMERICA & MEXICO

CHIP EXPRESS CORPORATION

Josh Bellin
2903 Bunker Hill Lane Suite 105
Santa Clara, CA 95054
USA
Tel: 408-988-2445 x176
Fax: 408-988-2449
email: joshb@chipx.com

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Lam Soon Ind. Building
SINGAPORE 2366
Tel: 65-769-1118
Fax: 65-769-2221
Ms. Nicole Ho, Sr. Sales & Marketing Engineer
email: maxmega@singnet.com.sg

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